Mathematical analysis of random telegraph noise in low-power applications of MOSFETs

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***Abstract*—Silicon MOSFETs are active switching elements which form the basis for most currently available digital circuits. Especially in information technology the growth in circuit complexity and data throughput leads to an increase in power consumption. For this reason, the energy efficiency of transistors has become a major design issue. A common way to increase the energy efficiency of these devices is to reduce the signal level, which finally leads to the so-called sub-threshold operation. An advantage of this approach is that it can be applied to common structures so that new device concepts are not necessarily required. However, the reduction in the signal level leads unavoidably to a degradation of the signal to noise ratio. Especially random telegraph noise has a significant influence on the circuit behavior. In this work this type of noise is studied mathematically. A stochastic simulation model was developed and a method was provided by which it can be determined how low the supply voltage can be chosen in order to keep the noise influence sufficiently low.**

I. Introduction

The infrastructure of information and communication technology (ICT) is continuously growing to satisfy the increasing demands of computation power, data transfer rate and memory requirements. An actual study of the Fraunhofer Institute [1] evaluated an energy consumption of the ICT in Germany of 10% of the overall consumption and it estimated an increase within the next 10 years of up to 20%. Consequently, the energy efficiency becomes an important design issue for the hardware of ICT.

CMOS transistors are the basic elements for digital data processing in the most components of ICT. Nowadays, a single chip can contain up to $5{\cdot}10^9$ of these elements. Hence, a minor reduction of the switching power of the single transistor has a big impact on the overall power consumption of the chip. A common way to reduce the switching power is the reduction of the structure size to minimize parasitic capacitances resulting in lower energy losses during the toggling between on and off state of the transistor. The actual structure size of a fabrication technology reaches 22nm [2]. Each further reduction is combined with huge investment costs for the facility and the development of new fabrication techniques.

Another option is to lower the voltage difference between on and off state leading to the so call sub-threshold operation. This method enables a very low power consumption without the necessity of new and cost-intensive fabrication technologies.

A consequence of this approach is, that different noise sources have an increased impact on the circuit behavior. In this respect, the so called random telegraph noise (RTN) plays a decisive role [3]. It is caused by trapping of single charge carriers on the boundary layer between gate oxide and channel. This results in a random toggling of the drain current between two fixed levels at a constant gate voltage.

In this work, a stochastic model was developed in order to analyze the influence of RTN on the drain current for various system parameters. Furthermore, a formula was provided in order to calculate the lowest supply voltage which ensures a 3σ stability margin.

II. Modelling of RTN

A. Definitions

We limited the analysis to nMOSFETs. The relevant parameters are the gate voltage V_G, the drain voltage V_D, the threshold voltage V_T, the drain current I_D, the threshold current I_T, the sub-threshold slope S, and the channel size, which is defined by length L and width W.

The RTN can be defined by the difference between both current levels, which we call RTN amplitude ΔI_D and the probability of a trapped electron, which we call RTN probability p. This probability is supposed to be constant for the whole gate voltage range.

The transfer function of a MOSFET in sub-threshold range can be calculated by [4]:

$$I_D = I_T \cdot \exp\left\{\ln(10)\frac{V_G - V_T}{S}\right\}\left(1 - \exp\left\{-\frac{qV_D}{kT}\right\}\right). \quad (1)$$

The threshold current depends on the channel size: $I_T = \alpha\frac{W}{L}$, where α is an appropriate parameter.

The off and on state of the transistor can be defined as two points on the transfer funktion V_G^{off} and V_G^{on}. V_G^{off} has to be a very small voltage or zero and V_G^{on} is a value in the sub-threshold range in the current analysis. The corresponding currents I_D^{off} and I_D^{on} can be calculated easily by using equation (1).

Then the state probabilities P^{off} and P^{on} can be defined:

$$P^{on} = \begin{cases} 0 & ,I_D \leq I_D^{off} \\ \frac{I_D - I_D^{off}}{I_D^{on} - I_D^{off}} & ,I_D^{off} < I_D < I_D^{on} \\ 1 & I_D \geq I_D^{on} \end{cases}, \quad P^{off} = 1 - P^{on}. \tag{2}$$

They give information about the probability with which the respective state of the transistor can be predicted. This way, the certainty of the states can be determined.

B. Stochastic simulation model

In the work of Ohata et al. [5] it is described that RTN is caused by a hole in the channel with a certain radius l. They analyzed the worst case scenario where this hole is located centered in the channel boundary layer and found a relation between the ratio of RTN amplitude and drain current (RTN ratio) and the hole radius:

$$\frac{\Delta I_D}{I_D} = \frac{4l^2}{WL - 2l(L - 2l)}. \tag{3}$$

This means that, with knowledge about the RTN amplitude, the size of the hole can be determined. Cheung et al. [6] confirmed equation (3) by measurements for various gate overdrives $(V_G - V_T)$ in sub-threshold near-threshold and super-threshold range. They measured the RTN ratio and calculated the hole radius l which is decreasing exponentially depending on the gate overdrive.

It is our goal to derive a design expression for the RTN amplitude depending on the system and operation conditions. For this reason, we used the above mentioned relationships in order to determine a fit function. First, we introduce dimensionless variables. All length variables are normalized ly $\Delta l = 1$nm and all voltages are normalized by $\Delta V = 1$mV. All normalized variables are marked by a bar. We found as a fit function

$$\bar{l} = 12.7 \cdot \exp\left\{-0.005(\bar{V_G} - \bar{V_T})\right\}. \tag{4}$$

Under the assumption that this dependence of the hole size on the gate overdrive is similar for all nMOSFETs, the RTN amplitude of arbitrary nMOSFETs can be calculated as a function of the channel size and the gate overdrive:

$$\Delta I_D = \frac{50.8 \cdot I_D \cdot \exp\left\{-0.01(\bar{V_G} - \bar{V_T})\right\}}{\bar{W}\bar{L} - 25.4 \cdot \exp\left\{-0.005(\bar{V_G} - \bar{V_T})\right\}} \times \cdot \frac{1}{(\bar{L} - 25.4 \cdot \exp\left\{-0.005(\bar{V_G} - \bar{V_T})\right\})} \tag{5}$$

C. Analytical determination of minimum supply voltage

A significant challenge for low-power applications of transistors is the determination of the optimum operating point. This means the supply voltage should be as low as possible and the state of the transistor is to be determined with a given accuracy, despite the noise impact. A common safety margin is assumed to be 3σ (see [7]).

In order to calculate this margin, the existence of a trap can be interpreted as binomially distributed random experiment, where p is the success probability in one trial, i.e. the RTN probability. The number of trials is named n. Then the mean value of this distribution can be calculated by $\mu = n \cdot p$ and the variance is $\sigma^2 = n \cdot p \cdot (1 - p)$. Multiplying μ by the RTN amplitude ΔI_D leads to the mean noise influence. Hence, the mean noisy drain current I_D^{RTN} in case of a negative trap, as it occurs in nMOSFETs, can be calculated by:

$$I_D^{RTN} = I_D - p \cdot \Delta I_D. \tag{6}$$

The corresponding current variance for a single trial is

$$\sigma_{I_D}^2 = \Delta I_D \cdot p \cdot (1 - p). \tag{7}$$

To realize a correct state determination, the safety margin can be calculated by using ΔI_D from equation (5) in

$$3\sigma = 3\sqrt{p \cdot (1 - p)}\sqrt{\Delta I_D}. \tag{8}$$

III. Conclusion

For sub-threshold operation there is a tradeoff between operational reliability and power consumption.

Two analytical methods were provided in order to evaluate the influence of RTN on the operation of MOSFETS in sub-threshold range and to determine the optimum supply voltage for low-power applications.

These methods enable the optimization of system parameters, like channel size and sub-threshold slope,with respect to the noise influence.

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