Design of Current-Controlled Current Conveyor Stage With Systematic Current Offset Reduction

Roman Sotner, Roman Prokop, Jan Jerabek, Vilem Kledrowetz, Lukas Fujcik
Faculty of Electrical Engineering and Communication
Brno University of Technology
Brno, Czech Republic
sotner@feec.vutbr.cz

Tomas Dostal
Dept. of Electrical Engineering and Computer Science
College of Polytechnics Jihlava
Jihlava, Czech Republic
tomas.dostal@vspj.cz

***Abstract* – This contribution presents modification of current-controlled current conveyor (CCCII) designed in order to reduce the systematic DC current offset of transfer between X and Z terminal and also an example of practical design including practical guideline and recommendations. Simulations in Cadence Spectre simulator with ON Semiconductor/AMIS I2T100 based on 0.7 µm technology CMOS07 were provided for verification of discussed features.**

Keywords-CCCII; CMOS; current conveyor; electronic control; offset reduction

I. INTRODUCTION

Current conveyors (CC) [1]-[4] have attracted attention of researchers for many years. There are many interesting modifications of basic structures defined by Sedra et al. [1]. However, elementary definitions [1]-[4] does not suppose any kind of electronic control of any parameter of the circuit. Several modifications were introduced in order to improve electronic controllability of their parameters. Intrinsic small-signal resistance of the current input terminal X (R_X) is the parameter which was explored in applications of so-called current controlled current conveyor of second generation (CCCII) [4]-[7]. An attention was also focused on current gain control between X and Z terminal (B) [8]-[10] in so-called electronically controllable current conveyor (ECCII). Many interesting conceptions followed, where combined methods of two parameters control were solved. Minaei et al. [11] introduced CMOS ECCII with independent electronic control of R_X and B. Similarly Kumngern et al. [12] defined control of these parameters in simple bipolar solution of the CC. De Marcellis et al. [13] contributed with voltage gain control (A). These ideas were also utilized in further complex elements for example in advanced current feedback amplifiers [14]-[15].

Unfortunately, many of the presented solutions were designed only for computer analysis and do not solve some practical requirements, e.g. minimization of DC offset and appropriate DC accuracy (very small transistors are used, which cause unacceptable matching offset and too low dynamic impedance in some cases). Our solution supposes practical utilization of the CC, expects practical design and later silicon implementation. Our circuit has very good accuracy of the current transfers and significantly improved (decreased) systematic DC current offset between X and Z terminal in frame of CCCII (controllable R_X), which is always present.

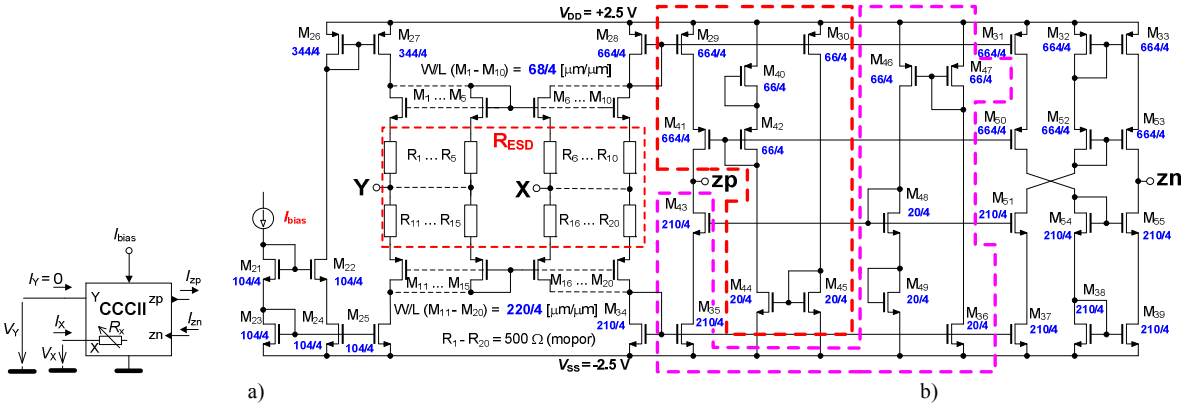

Figure 1. Current-controlled currrent conveyor (CCCII) with systematic DC current offset reduction: a) schematic symbol, b) cell structure.

Research described in this paper was financed by Czech Ministry of Education in frame of National Sustainability Program under grant LO1401. For research, infrastructure of the SIX Center was used. Research described in the paper was supported by Czech Science Foundation project under No. 14-24186P. Grant No. FEKT-S-14-2281 also supported this research. The support of the project CZ.1.07/2.3.00/20.0007 WICOMT, financed from the operational program Education for competitiveness, is gratefully acknowledged.

ISBN 978-80-261-0386-8, © University of West Bohemia, 2015

Schematic symbol and internal structure of the CCCII cell with improved features are shown in Fig. 1. Definition of the CCCII behavior is well known [4]-[7]: $V_X = V_Y + R_X I_X$, $I_Y = 0$, $I_{zp} = -I_{zn} = I_X$.

II. Design of the CCCII Cell

We have used ON Semiconductor/AMIS I2T100 fabrication technology available in frame of Europractice academic consortium. This technology is precise, verified and perfect for similar analog and mixed-mode designs. In case of smaller technologies, we always have to design W and L dimensions large enough for sufficient DC accuracy in the case of analog circuits. Thus, simply put, when only analog design is considered, there is usually no point in using smaller technology (benefit vs. cost is usually not balanced).

The CCCII contains three main subparts. The first of them is biasing circuit (M_{21-27}). This part has to provide bias current for the rest of the structure. Design of this section was provided by following specifications: overdrive voltage $\Delta V_{GS} = V_{Dsat} = V_{GS} - V_{th} = 0.4$ V (where V_{th} is threshold voltage: 0.74 V for NMOS and 1.1 V for PMOS typically), we can use larger ΔV_{GS} because there is not amplitude swing (signal) and voltage space given by supply voltage corners ($V_{DD} = -V_{SS} = 2.5$ V) is sufficient, this fact also reduces overall W/L ratio of transistors (better noise features, saving of the chip area); maximal bias current $I_{bias} = 200$ µA; length of transistors $L = 4$ µm was chosen for sufficiently high MOS output resistance. Transconductance parameters (fabrication constants given by gate-oxide capacitance and mobility of carriers) for hand calculations are approximately $K_{pN} = 95$ µA/V^2 and $K_{pP} = 29$ µA/V^2. Based on equations [16]:

$$W_{M21-25} = \frac{2I_{bias}}{K_{pN}\left(V_{GS\_M21-25} - V_{thN}\right)^2} L, \qquad (1)$$

$$W_{M26-27} = \frac{2I_{bias}}{K_{pP}\left(V_{GS\_M26-27} - V_{thP}\right)^2} L, \qquad (2)$$

we calculated widths: $W_{M21-25} = 105$ µm and $W_{M26-27} = 345$ µm.

The second part is so-called translinear section [5], [17]-[19], where we suppose R_X control. Generally known CCCII contains only four transistors (2 NMOS and 2 PMOS) in translinear section. However, we have to match recommended ESD requirements. Therefore, this part consists of ten "fingers" M_{1-10} and M_{11-20} where additional resistors R_{1-20} are required due to the ESD protection of the inputs. Unfortunately, resistance (500 Ω) of R_{6-10} and R_{16-20} directly influences overall value of the R_X. This additional resistance is noted as R_{ESD} in further text. Overall value of small-signal R_X can be expressed as:

$$R_X \cong \frac{0.2}{\frac{1}{R_{ESD} + 1/g_{mP}} + \frac{1}{R_{ESD} + 1/g_{mN}}}, \qquad (3)$$

where

$$g_{mP} = \sqrt{2K_{pP}\left(\frac{W}{L}\right)_P 0.2I_{bias}}, \; g_{mN} = \sqrt{2K_{pN}\left(\frac{W}{L}\right)_N 0.2I_{bias}}. \quad (4),(5)$$

Parameters g_{mP} and g_{mN} are partial transconductances of the single finger (M_{6-10}, M_{16-20}). Constant 0.2 in (3)-(5) is given by division of R_X to five fingers (I_{bias} is also divided to five branches). We expect $g_{mP} = g_{mN} = g_{mNP}$ for simple design of R_X value. Then, we can simplify (3) to form:

$$R_X \cong 0.1 \cdot \left(R_{ESD} + 1/g_{mNP}\right). \qquad (6)$$

We can express direct relation for W/L ratio of partial finger NMOS (M_{1-10}) and PMOS (M_{11-20}) as:

$$\left(\frac{W}{L}\right)_{N,P} = \frac{1}{2K_{pN,P}0.2I_{bias}}\left(\frac{1}{\frac{R_X}{0.1} - R_{ESD}}\right)^2. \qquad (7)$$

Design requirements are: maximal $I_{bias} = 200$ µA (40 µA in each of 5 branches); $R_{ESD} = 500$ Ω; $R_X = 330$ Ω, $L = 4$ µm. We calculated $W_{M11-20} = 220$ µm (PMOS) and $W_{M1-10} = 67$ µm (NMOS) from (7). Supposing typical $\Delta V_{GS} = 0.25$ V (this part is processing signal with amplitude swing, we cannot allow bigger value of ΔV_{GS}), we verified that transistors should operate in saturation up to $I_{bias} = 50$ µA in each finger (for $\Delta V_{GS} = 0.25$ V), calculated from equation [16]:

$$I_{bias} = \frac{K_{pN,P}}{2}\left(\frac{W}{L}\right)_{N,P}\left(\Delta V_{GS}\right)^2. \qquad (8)$$

Our design supposes I_{bias} should reach 40 µA in each finger for $R_X = 330$ Ω.

The last part of the CCCII contains output section (mirrors) with DC current offset reduction auxiliary circuits. We used the same equations (1) and (2) for calculation of dimensions of the main transistors of the output section, similarly as at the beginning of our discussion (we suppose $\Delta V_{GS} = 0.29$ V, $L = 4$ µm). We obtained from the calculation $W_{M34,35,37,38,39,43,51,54,55} = 200$ µm, $W_{M28,29,31,32,33,41,50,52,53} = 656$ µm. Explanation of the auxiliary circuits design is given in following section.

III. DC Current Offset Reduction

Standard cascoding of CMOS current mirrors [16] is very well-known method how to increase output resistance of the current mirror in order to ensure high accuracy of mirroring. However, there are situations where standard approach cannot be applied due to limited voltage space in the structure. Fortunately, there are some methods (different way of cascode biasing), that can be very useful in particular solutions. We used auxiliary networks (red- and pink-colored parts) in our solution of the CCCII (Fig. 1). Partial schematic diagram of the auxiliary circuit for current offset reduction between X and zp, zn terminals is shown in Fig. 2b (for half of the section, the second part is analogical). The circuit operation is based on additional supporting MOS transistor connected to the output drive. It works very similarly as standard cascoding (Fig. 2a) of current mirrors [16] but this

arrangement does not consume so large voltage space in translinear loop as standard cascoded current mirror.

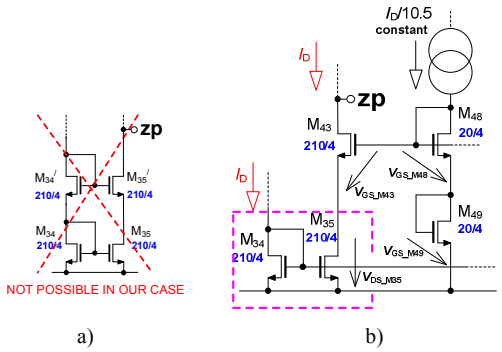

Figure 2. Basic principle of static DC current offset reduction: a) standard cascoding, b) cascoding with different way of biasing.

Our goal is to design current mirror M_{34}, M_{35} (and others if more outputs of this mirror are required) with very accurate relation (unity gain in our case) between input and output current to minimize systematic DC offset. Therefore, V_{DS} of both transistors must be almost equal. We will suppose constant bias current I_{bias} (fixed R_X value) in the first case of our discussion. Auxiliary network (M_{43}, M_{48}, M_{49}) of the output drive provides following relation:

$$V_{GS\_M43} + V_{DS\_M35} = V_{GS\_M48} + V_{GS\_M49}. \quad (9)$$

Additional section sufficiently increases output impedance of the mirror. Thus, voltage drop across V_{DS_M35} is almost equal to voltage drop across diode M_{34} (if W/L and drain currents of M_{49} and M_{34} are identical then $V_{GS\_M34} = V_{DS\_M35} = V_{GS\_M49}$). Very similar situation (well-known fact) occurs in case of constant ratio of current through branch M_{48} and M_{49} (diodes) and current through M_{34}, M_{35}, M_{43} ($k_1 = I_{D\_M34,35,43}/I_{D\_M48,49}$) and aspect ratios W/L of M_{43}, M_{35}, M_{48} and M_{49} ($k_2 = (W/L_{M34,35,43})/(W/L_{M48,49})$). We obtained:

$$V_{DS\_M35} = V_{GS\_M34} = V_{GS\_M49} = \sqrt{\frac{2I_D}{k_1}\left(K_{pN}\frac{\left(\frac{W}{L}\right)_{M49}}{k_2}\right)^{-1}} + V_{th\_N}, \quad (10)$$

where we can see that this V_{GS} is not dependent on k if W/L and current gain of the mirror are designed as equal ($k_1 = k_2 = k$).

Above discussed system for DC offset reduction works properly if constant I_D is available. However, additional circuitry is required to ensure sufficiently low offset also if biasing conditions are changed. We suppose intentional control of I_{bias} in order to adjust R_X value. The current through branch M_{48} and M_{49} (I_D/10.5) should be also adjusted in accordance with I_{bias} (I_D in explanatory Fig. 2b and Fig. 3). Otherwise, V_{GS_M48} and V_{GS_M49} are not changed simultaneously with others – directly influenced by I_D. Thus, V_{DS_M35} is not almost equal to V_{GS_M34} for large changes of I_D anymore (offset increases in specific range of I_{bias} adjusting) and transistors may even left their operation region (saturation) in the worst case. Additional current mirrors (M_{34}-M_{36}, M_{46}-M_{47}) in Fig. 3 solve this problem partially. It seems to be sufficient solution in required range of I_{bias} adjusting. Our design example supposes 10.5-times smaller transistors of auxiliary network (M_{46}, M_{47}, M_{48}, M_{49}, M_{36}) to save chip area. For additional information see comparison of the simulation results (Fig. 5) based on CCCIIs utilized solutions in Fig. 2b and Fig. 3.

Calculated W/L ratios together with final W/L (see Fig. 1) modified in accordance to the precise layout guidelines (division of active areas of transistors to fingers, matching-interdigitation, dummy, ESD recommendations, etc. [16]) are summarized in Tab. 1.

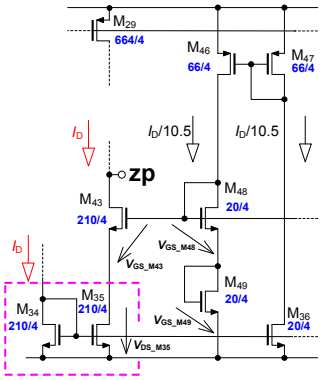

Figure 3. Principle of DC current offset reduction with dynamical response on bias current changes.

TABLE I. CALCULATED AND FINAL W/L RATIOS

Transistor	W/L ratio [-]	
	calculated	***final***
$M_{1\text{-}10}$	67/4	**68/4**
$M_{11\text{-}20}$	**220/4**	
$M_{21\text{-}25}$	105/4	**104/4**
$M_{26\text{-}27}$	345/4	**344/4**
$M_{28,29,31,32,33,41,50,52,53}$	656/4	**664/4**
$M_{34,35,37,38,39,43,51,54,55}$	200/4	**210/4**
$M_{30,40,42,46,47}$	**66/4**	
$M_{36,44,45,48,49}$	**20/4**	

IV. SIMULATION RESULTS

Detail of the DC transfer characteristic between X and zp (zn) terminals for standard CCCII (without offset reduction) and CCCII presented in Fig. 1 is shown in Fig. 4.

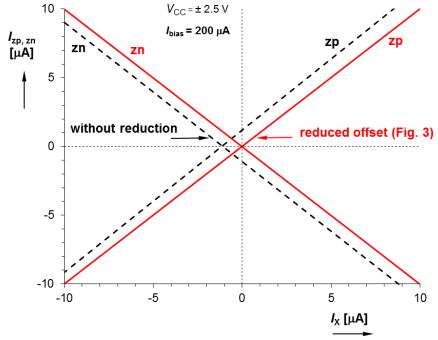

Figure 4. Detail of DC transfer between X and zp, zn terminals.

We analyzed the systematic DC current offset of the standard CCCII topology without offset minimization (for our design parameters). Figure 5 indicates dependence of this DC offset on I_{bias} adjusted from 1 µA to 200 µA. The smallest value of the DC offset of the standard CCCII (without reduction) achieves about 50 nA (I_{bias} = 1 µA but all transistors of CCCII are not operating in saturation regime anymore) and the highest value is 1.15 µA (200 µA). The solution with reduced offset (Fig. 3) offers values 0.66 – 20 nA in discussed I_{bias} range. Dependence of small-signal R_X

on I_{bias} in the same range is shown in Fig. 6. Theoretical (ideal) trace was achieved from (3)-(5). Simulated value $R_X = 306\ \Omega$ for $I_{bias} = 200\ \mu A$ was obtained. Hand calculation gives value 330 Ω. AC responses of the transfer between X and zp and zn terminals are in Fig. 7 (18.5 and 12.1 MHz -3 dB bandwidths were achieved for $I_{bias} = 200\ \mu A$).

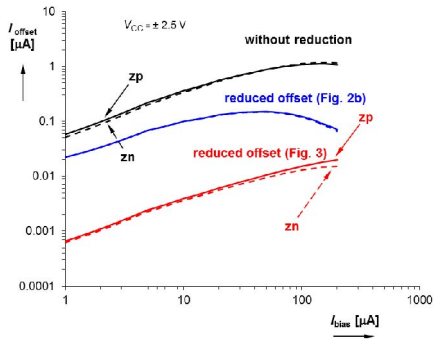

Figure 5. Dependence of current offset value on I_{bias} adjusting.

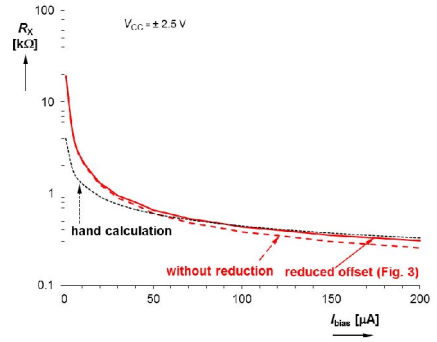

Figure 6. Dependence of R_X on I_{bias} adjusting.

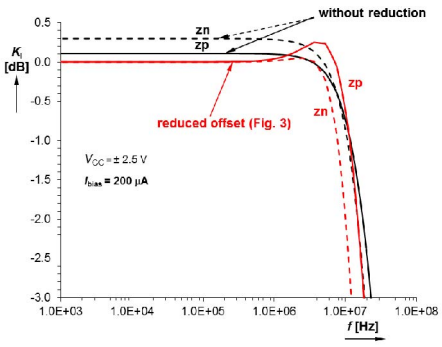

Figure 7. AC transfer between X and zp, zn terminals.

V. Conclusion

We have discussed solution how to improve DC accuracy of the standard CMOS CCCII. DC offset of the transfer between X and zp or zn terminals can be significantly reduced (from 1.15 µA in basic CCCII to 20 nA in variant with systematic offset reduction for the highest value of the $I_{bias} = 200\ \mu A$). It is worth to solve the systematic offset reduction because matching offset analysis (CCCII with or without systematic offset reduction) revealed comparable offset dispersions (sigma around 1 µA) to unreduced systematic value. Our topology improves also accuracy of the unity current transfer significantly (Fig. 7). Our future work expects analysis of fabricated prototype.

References

[1] A. Sedra, K. C. Smith, "A second generation current conveyor and its applications," IEEE Transaction on Circuit Theory, vol. CT-17, no. 2, pp. 132-134, 1970.

[2] J A. Svoboda, L. Mcgory, S. Webb, "Applications of commercially available current conveyor," Int. Journal of Electronics, vol. 70, no. 1, pp. 159-164, 1991.

[3] H. Barthelemy, M. Fillaud, S. Bourdel, J. Gaunery, "CMOS inverters based positive type second generation current conveyors," Analog Integrated Circuits and Signal Processing, vol. 50, no. 2, pp. 141–146, 2007.

[4] D. Biolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: Classification, Review, and New Proposal," Radioengineering, vol. 17, no. 4, pp. 15–30, 2008.

[5] A. Fabre, O. Saaid, F. Wiest, C. Boucheron, "High frequency applications based on a new current controlled conveyor," IEEE Trans. on Circuits and Systems - I, vol. 43, no. 2, pp. 82–91, 1996.

[6] S. B. Salem, M. Fakhfakh, D. S. Masmoudi, M. Loulou, P. Loumeau, N. Masmoudi, "A high performance CMOS CCII and high frequency applications," Analog Integrated Circuits and Signal Processing, vol. 49, no. 1, pp. 71–78, 2006.

[7] I. Eldbib, V. Musil, "Self-cascoded Current Controlled CCII Based Tunable Band Pass Filter," in Proc. 18th Int. Conf. Radioelektronika, Praha, 2008, pp. 1–4.

[8] W. Surakampontorn, W. Thitimajshima, "Integrable electronically tunable current conveyors," IEE Proceedings-G, vol. 135, no. 2, pp. 71-77, 1988.

[9] W. Surakampontorn, K. Kumwachara, "CMOS-based electronically tunable current conveyor," Electronics Letters, vol. 28, no. 14, pp. 1316-1317, 1992.

[10] A. Fabre, N. Mimeche, "Class A/AB second-generation current conveyor with controlled current gain," Electronics Letters, vol. 30, no. 16, pp. 1267-1268, 1994.

[11] S. Minaei, O. K. Sayin, H. Kuntman, "A new CMOS electronically tunable current conveyor and its application to current-mode filters," IEEE Trans. on Circuits and Systems - I, vol. 53, no. 7, pp. 1448–1457, 2006.

[12] M. Kumngern, S. Junnapiya, "A sinusoidal oscillator using translinear current conveyors," in Proc. Asia Pacific Conference on Circuits and Systems (APPCAS), Kuala Lumpur, 2010, pp. 740–743.

[13] A. Marcellis, G. Ferri, N. C. Guerrini, V. Scotti, A. Trifiletti, "The VGC-CCII: a novel building block and its application to capacitance multiplication," Analog Integrated Circuits and Signal Processing, vol. 58, no. 1, pp. 55–59, 2009.

[14] R. Sotner, J. Jerabek, N. Herensar, T. Dostal, K. Vrba, "Electronically adjustable modification of CFA: Double Current Controlled CFA (DCC-CFA)," in Proc. 35th Int. Conf. on Telecommunications and Signal Processing (TSP2012), Prague, 2012, pp. 401-405.

[15] R. Sotner, N. Herencsar, J. Jerabek, R. Dvorak, A. Kartci, T. Dostal, K. Vrba, "New double current controlled CFA(DCC-CFA) based voltage-mode oscillator with independent electronic control of oscillation condition and frequency," Journal of Electrical Engineering, vol. 64, no. 2, pp. 65-75, 2013.

[16] B. Razavi, Design of analog CMOS integrated circuits, New York, McGraw-Hill, 2001.

[17] B. Gilbert, "Translinear Circuits: a Historical Overview," Analog Integrated Circuits Signal Processing, vol. 9, no. 2, pp. 95-118, 1996.

[18] A. Bradley, "MOS Translinear Principle for All Inversion Levels," IEEE Trans. on Circuits and Systems–II: vol. 55, no. 2, pp. 121-125, 2008.

[19] R. Prokop, V. Musil, "Modular approach to design of modern circuit blocks for current signal processing and new device CCTA," Seventh International Conference on Signal and Image Processing (IASTED 2005), Honolulu, 2005, pp. 494-499.