Dynamic Duty-cycle Limitation of the Boost DC/DC Converter allowing Maximal Output Power Operations

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Abstract—This paper describes the concept of the dynamic duty-cycle limiter of the boost dc-dc converter. Duty-cycle limitation in boost converters is usually used to protect the bottom switch against an excessive current, and also to avoid instability occurring at high duty-cycle operations. Compared to fixed limitation, dynamic limiter enables to detect and maintain maximal possible output voltage $V_{\text{MAX}}$, when desired output voltage cannot be provided e.g. due to excessive load current or increased resistance of the switches. This feature allows to extend the operation range of the converter and powered device. Developed method applies to low power converters, and it is based on the power balance condition detection circuit. This detection is realized via simple and low consumption voltage sensing. Paper presents description of the method, circuit implementation and shows simulated results obtained with integrated 0.13μm CMOS boost dc-dc converter.

I. INTRODUCTION

Boost converter is a non-isolated power converter that may be used when a higher output voltage than the one provided by the input source is required. It contains two power switches, one inductor and an output capacitor. For an ideal converter ($R_{\text{COLL}}, R_{\text{LOW}},$ and $R_{\text{HIGH}} = 0$), the output voltage can be determined by the volt-second balance as a function of the input voltage $V_{\text{IN}}$ and duty-cycle $D$ [1]:

$$V_{\text{OUT}} = \frac{V_{\text{IN}}}{1-D}$$  \hspace{1cm} (1)

The inductor (or input) current can be obtained as function of the load and duty-cycle:

$$I_{\text{COLL}} = \frac{V_{\text{IN}}}{R_{\text{S}} (1-D)^2} = \frac{I_{\text{OUT}}}{1-D}$$  \hspace{1cm} (2)

For ideal boost converter, a zero duty-cycle $D$ provides $V_{\text{OUT}} = V_{\text{IN}}$, whereas for $D \rightarrow 1$ results in infinite output voltage $V_{\text{OUT}}$, and also infinite inductor current $I_{\text{COLL}}$. Compared to ideal $V_{\text{OUT}}$ (1), real converter produces lower output voltage for the same duty-cycle. This limitation can be demonstrated by the circuit of real boost converter Fig. 1 a). This converter contains inductor and switches parasitic resistances $R_{\text{COLL}}, R_{\text{BOT}}$ and $R_{\text{HIGH}}$. At high output current, these resistances are responsible for dominant power loss of the converter [1]. Steady-state output voltage $V_{\text{OUT}}$ of real boost converter can be obtained by the help of averaged model shown in Fig. 1 b). Here, technique of linearization [2], [4] employing controlled sources was used. DC analysis of this model allows to obtain the output voltage as:

$$V_{\text{OUT}} = \frac{R_{\text{S}} (1-D) V_{\text{IN}}}{D^2 R_{\text{L}} - D (2R_{\text{L}} + R_{\text{HIGH}} - R_{\text{LOW}}) + R_{\text{L}} + R_{\text{HIGH}} + R_{\text{COLL}}}$$  \hspace{1cm} (3)

The reduction of the output voltage is demonstrated for various load resistances $R_{\text{LOAD}}$ in Fig. 2. $V_{\text{OUT}}/V_{\text{IN}}$ conversion characteristics with $R_{\text{LOAD}} < \infty$ contains three significant areas:

1) $D < D_{\text{CRIT}}$: normal operations with positive gain, where characteristic is close to ideal Eq.(1),

2) $D = D_{\text{CRIT}}$: providing maximum output voltage $V_{\text{MAX}}$,

3) $D > D_{\text{CRIT}}$: negative gain area, where the output voltage decrease with increasing duty-cycle.

In normal mode of the feedback regulation, the control loop maintains the desired output voltage, and converter operates below the critical duty-cycle $D_{\text{CRIT}}$. However, due to e.g. high load current, insufficient input power, or increase of the converter switches resistance (due to the temperature increase, or by the drop of the MOSFET switch gate-source voltage), $V_{\text{OUT}}$ can decrease below desired value (1), and the feedback loop saturates. In an extreme scenario, controller increases the duty-cycle $D$ above $D_{\text{CRIT}}$ and the conversion gain $V_{\text{OUT}}/V_{\text{IN}}$ becomes negative. Beyond the loop instability, high duty-cycle operation leads to excessive inductor current (2) and potential damage of the bottom switch.
The value of critical duty cycle \( D_{\text{CRIT}} \) can be obtained by setting the 1° derivative \( \frac{d(V_{\text{OUT}})}{dD} = 0 \) as:

\[
D_{\text{CRIT}} = 1 - \sqrt{(R_{\text{COIL}} + R_{\text{LOW}})/R_I} \tag{4}
\]

and is independent on \( R_{\text{HIGH}} \) (\( R_{\text{HIGH}} \) can be seen as a part of the load).

In order to avoid the gain polarity inversion and also the excessive inductor current \( I_{\text{COIL}} \), duty-cycle is usually clamped to a fixed value \( D_{\text{MAX}} \) [1], [3]. This maximal duty-cycle is designed in a way to always maintain positive conversion gain, e.g. \( D_{\text{MAX}} < 0.67 \) in Fig. 2. However, in normal regulation mode (where duty-cycle limitation is not required), fixed value \( D_{\text{MAX}} \) can reduce the output voltage range. As example, \( D_{\text{MAX}} = 0.67 \) from Fig. 2 clamps the maximal output voltage to 2.4V when \( R_{\text{LOAD}} = 40\Omega \). By setting \( D_{\text{MAX}} = 0.83 \), the converter can provide \( V_{\text{OUT}} = 3\text{V} \) for \( R_{\text{LOAD}} = 40\Omega \), or even \( V_{\text{OUT}} = 5.2\text{V} \) at \( R_{\text{LOAD}} = \infty \).

In this paper, concept of the dynamic duty-cycle limitation is described. Presented circuit allows to automatically determine the optimal duty-cycle \( D_{\text{CRIT}} \) for wide range of load, switch and inductor resistances. The dynamic limitation is based on the power balance concept presented in section II. Implementation of the critical duty-cycle detection circuit is described in section III, whereas feedback loop circuit allowing dynamic (real-time) limitation is described in section IV. This section also present results obtained by the post-layout simulations of the integrated CMOS converter.

II. POWER BALANCE METHOD

In linear circuits, maximal power that can be transferred from a voltage source \( V_0 \) with output resistance \( R_{\text{OUT}} \) is obtained, when \( R_{\text{OUT}} \) is matched to the load resistance, i.e. \( R_{\text{OUT}} = R_{\text{LOAD}} \). In this case, \( P_{\text{LOSS}} \) dissipated on the source resistance is equal to the power \( P_{\text{LOAD}} \) delivered to the load:

\[
P_{\text{LOSS}} = P_{\text{LOAD}} \tag{5}
\]

The output resistance \( R_{\text{OUT}} \) of the boost converter can be obtained by DC analysis of the linear model Fig. 1 b) described in [4]:

\[
R_{\text{OUT}} = \frac{R_{\text{COIL}} + (1-D)R_{\text{HIGH}} + DR_{\text{LOW}}}{(1-D)^2} \tag{6}
\]

where the output resistance increase with duty-cycle ratio. The \( R_{\text{OUT}} \) allows us to rewrite the output voltage (3) as \( V_{\text{OUT}} = V_0 - R_{\text{OUT}}R_{\text{LOAD}} \). Here, \( V_0 \) corresponds to ideal output voltage (1).

As already mentioned, the maximal power transfer theorem (5) applies for linear circuits only. This signifies, that \( R_{\text{OUT}} \) (but not \( R_{\text{LOAD}} \)) should be constant, independent on the load current. However, inserting \( D_{\text{CRIT}} \) into (6), result in \( R_{\text{OUT}(\text{CRIT})} \) being a function of \( R_{\text{LOAD}} \), and thus of the output current \( I_{\text{LOAD}} \):

\[
R_{\text{OUT}(\text{CRIT})} = R_L + \sqrt{R_L \cdot \frac{(R_{\text{HIGH}} - R_{\text{LOW}})}{\sqrt{R_{\text{COIL}} + R_{\text{LOW}}}}} \tag{7}
\]

A condition of linearity of \( R_{\text{OUT}(\text{CRIT})} \) can be derived from equation \( R_{\text{OUT}(\text{CRIT})} = R_L \) resulting in:

\[
R_{\text{LOW}} = R_{\text{HIGH}} = R_{\text{SW}} \tag{8}
\]

In other words, when \( R_{\text{LOW}} = R_{\text{HIGH}} \), \( R_{\text{OUT}(\text{CRIT})} \) is constant and equal to \( R_I \). This corresponds to the condition of the impedance matching required by (5).

Fortunately, mismatch \( R_{\text{LOW}} \neq R_{\text{HIGH}} \) has very low impact to the maximum power point. This low sensitivity can be demonstrated by the plot shown in Fig. 3. Here, relative and absolute errors of \( V_{\text{OUT}} \) and \( D \) have been plotted in wide range as function of the ration \( R_{\text{HIGH}}/R_{\text{LOW}} \). It results, that approximate using of (5) can yield accurate optimum in a wide range of switch resistances.

![Fig. 2. \( V_{\text{OUT}}/V_{\text{IN}} \) DC voltage transfer function plotted of the real boost converter plotted by use Eq.(3).](Image)

![Fig. 3. Impact of mismatch \( R_{\text{HIGH}} \neq R_{\text{LOW}} \). Values \( D_{\text{CRIT}} \) and \( V_{\text{MAX}} \) are obtained by using ideal \( D_{\text{CRIT}} \) (4), whereas \( D_{\text{CRIT}}' \) and \( V_{\text{MAX}}' \) from use condition (5).](Image)

It is interesting to mention, that for a converter operating at \( D = D_{\text{CRIT}} \) (4), the inductor current has constant value \( I_{\text{COIL}(\text{CRIT})} \) which is independent on the load resistance \( R_{\text{LOAD}} \):

\[
I_{\text{COIL}(\text{CRIT})} = \frac{1}{2} \frac{V_{\text{IN}}}{R_{\text{COIL}} + R_{\text{SW}}} \tag{9}
\]

By regulating \( I_{\text{COIL}} \) to \( I_{\text{COIL(CRIT)}} \) (e.g. via duty cycle or load resistance value), maximal output power operation
can be obtained. However, this regulation would require an accurate knowledge and high time stability of $R_{COL}$, $R_{SW}$ and $V_{IN}$.

Next section presents an approach allowing to obtain the power balance condition (5) through simple and low consumption voltage sensing of the converter internal nodes.

III. CRITICAL DUTY-CYCLE DETECTION

In order to provide detection of the power balance condition (5), power dissipated in the converter and load resistances needs to be measured.

As shown in the converter schematic in Fig. 1 a), the inductor current is commutated between the low and high side switch resistances $R_{LOW}$ and $R_{HIGH}$ during $D$ and $(1-D)$ fraction of the period $T_{SW}$. Power dissipated in the converter structure can be then written as weighted contribution of $R_{LOW}$ and $R_{HIGH}$:

$$P_{LOS} = I^2_{COL} \left( R_{COL} + DR_{BOT} + (1-D)R_{UP} \right)$$  \hspace{1cm} (10)

The entire load current $I_{LOAD}$ is delivered through the high-side switch during $(1-D)$ portion of the period $T_{SW}$. Load power $P_{LOAD}$ from (5) can be then written as:

$$P_{OUT} = I^2_{COL} (1-D)V_{OUT}$$  \hspace{1cm} (11)

Comparing $P_{OUT}$ to (10) as required by power balance (5) results in:

$$I_{COL} (1-D)V_{OUT} = I^2_{COL} \left( R_{COL} + DR_{BOT} + (1-D)R_{UP} \right)$$  \hspace{1cm} (12)

Advantageously, squared values of $I_{COL}$ can be eliminated, which allows to obtain voltage equation:

$$(1-D)V_{OUT} = \frac{I_{COL}R_{COL} + I_{COL}R_{LOW} + I_{COL}R_{HIGH}(1-D)}{V_{IN}}$$  \hspace{1cm} (13)

In this equation, the right side represents the sum of average voltage drops on $R_{COL}$, $R_{LOW}$, and $R_{HIGH}$ whereas left side corresponds to the output voltage $V_{OUT}$ scaled (PWM modulated) by $(1-D)$.

A. Measurement of the Average Voltages

The boost converter with RC filter voltage sensing circuits is shown in Fig. 4. Here, measured average voltages indicated by the arrows correspond to terms mentioned in (13).

Typically, inductor current in CCM (continuous conduction mode) converter delivering high output current contains a DC component with a small triangular ripple part. Consequently, DC voltage $V_{COL_AVG}$ can be obtained by filtering inductor terminal voltage. This approach is frequently used in current sensing circuits such as [6]. Voltage across RC-filter capacitor $C_1$ is then $V_{COL_AVG} = I_{COL}R_{COL}$. Similarly, switch voltages $V_{LOW_AVG}$ and $V_{HIGH_AVG}$ are obtained by RC low-pass filters. In particular, $R_{LOW}$ and $R_{HIGH}$ are conducting the current $I_{COL}$ during $D$ and $(1-D)$ portion of the period, respectively. It results that $V_{LOW_AVG}$ and $V_{HIGH_AVG}$ are weighted by $D$ and $(1-D)$ terms as intended by (13). Compared to this, term $(1-D)V_{OUT}$ is obtained by PWM modulation and filtering of the output voltage $V_{OUT}$, but can also be generated from $V_{IN}(V_{IN} = (1-D)V_{OUT})$.

In order to compare left and right side of (13), three floating voltages are to be measured and added. Ideally, this would require at least three differential high-input impedance amplifiers.

B. Modified Power Balance Sensing Circuit

In order to simplify the circuit implementation of the power balance detection, Eq. (13) has to be rearranged. In particular, $R_{COL}$ can be split as:

$$I_{COL}R_{COL} = I_{COL}R_{COL}D + I_{COL}R_{COL}(1-D)$$  \hspace{1cm} (14)

Using this term in (13) reveals the power balance condition (5) to be:

$$(1-D)V_{OUT} = I_{COL} \left[ R_{COL}D + I_{COL}R_{COL} \right] + I_{COL} \left[ R_{COL}(1-D) \right]$$  \hspace{1cm} (15)

Here, terms with $D$ and $(1-D)$ can be collected:

$$(1-D)\left(V_{OUT} - I_{COL}R_{COL} - I_{COL}R_{SW} \right) = D \left(I_{COL}R_{COL} + I_{COL}R_{COL} \right)$$  \hspace{1cm} (16)

This equation allows us to realize the detection of the power balance condition (5) by measuring the average voltages $V_{(1-D)}$ and $V_{D}$, both referred to the ground. If $V_{(1-D)}$ and $V_{D}$ converter operates at the maximum possible output voltage, i.e. deliver maximal output power.

Schematic realization of (16) is shown in Fig. 5. The operation of this circuit can be described as follows: inductor RC filter capacitor $C_1$ is charged to DC voltage $R_{COL}I_{COL}$. During the low-side switch conduction phase $D$, current $I_{COL}$ creates voltage $I_{COL}R_{COL}$ on the low-side switch resistance. Thanks to conducting bottom switch $SW_{LOW}$, $C_1$ positive terminal (1) is at voltage $I_{COL}R_{COL}$. During this conduction phase, node (1) is connected to $R_A$ by PWM modulator A. During
opposite conduction phase \((1-D)\), RC filter input is connected to GND. This allows to obtain scaled DC voltage \(D\text{ICOL}(R_{\text{HIGH}}+R_{\text{COL}})\) from right-side of (16).

Obtaining the left side of (16) is more difficult. Here, voltage \(I_{\text{COL}}(R_{\text{COL}}+R_{\text{HIGH}})\) should be subtracted from \(V_{\text{OUT}}\) and weighted by \((1-D)\) term. This subtraction is realized by an additional switched-capacitor “inverter” circuit shown in Fig. 5. Voltage \(I_{\text{COL}}(R_{\text{COL}}+R_{\text{HIGH}})\) is generated during \((1-D)\) conduction phase by serial connection of \(C_1\), and voltage drop of the high-side switch voltage \(I_{\text{COL}}R_{\text{HIGH}}\) via \(S_{W_{\text{HIGH}}}\) Switches \((1-D)\) related to the inverter then allow to average and store this voltage in \(C_2\). During the complementary phase \(D\), inverter subtracts this voltage from \(V_{\text{OUT}}\) and stores the result in \(C_3\). Steady-state voltage of the node \((2)\) is \(V_{\text{OUT}}-I_{\text{COL}}(R_{\text{COL}}+R_{\text{HIGH}})\). Consequently, weighting by the term \((1-D)\) is provided by PWM modulator \(B\), and allows us to obtain the left side of (16).

Behavior of power balance sensing circuit from Fig. 5 is shown by the switched-mode simulation in Fig 6. Here, we notice that \(V_{\text{D AVG}}\) increases with increasing duty-cycle, whereas \(V_{\text{1-(D AVG)}}\) decreases.

\[\text{Fig. 6. Switched-mode simulation of the circuit from Fig. 5.}\]

Crossing point \(V_{\text{D AVG}} = V_{\text{1-(D AVG)}}\) then corresponds to peak voltage \(V_{\text{MAX}}\) (maximal output power), achievable by the converter for given operating point. Moreover, difference \(V_{\text{1-(D AVG)}} - V_{\text{D AVG}}\) allows to determine the gain of the critical duty-cycle limitation circuit, which is suitable for the synthesis of the feedback control transfer function of \(D_{\text{CRIT}}\).

As given by (5), operations at \(D = D_{\text{CRIT}}\) results in the power loss \(P_{\text{LOSS}}\) dissipated by the converter being equal to the power delivered to the load. As already mentioned, this limits the use of the dynamic duty-cycle limiter to the low-power converters.

IV. DYNAMIC DUTY-CYCLE LIMITER FEEDBACK LOOP

While the boost converter operates below critical duty-cycle \(D_{\text{CRIT}}\), feedback control loop (current or voltage mode) maintains the regulation of \(V_{\text{OUT}}\), and voltages \(V_{\text{1-(D AVG)}} > V_{\text{D AVG}}\). By e.g. increasing \(I_{\text{OUT}}\), \(V_{\text{1-(D AVG)}}\) and \(V_{\text{D AVG}}\) approach (see Fig. 6). Exceeding the critical duty-cycle \(D_{\text{CRIT}}\) results in \(V_{\text{1-(D AVG)}} < V_{\text{D AVG}}\) and in a decrease of \(V_{\text{OUT}}\) below required value. In this condition, the main feedback loop saturates. However, while \(V_{\text{1-(D AVG)}} < V_{\text{D AVG}}\) occurs, the dynamic duty-cycle limiter takes control over the main voltage regulation loop, and try to regulate \(V_{\text{1-(D AVG)}} = V_{\text{D AVG}}\). This allows the converter to operate with \(D_{\text{CRIT}}\,\text{and maintain } V_{\text{OUT}}\) at highest possible value \(V_{\text{MAX}}\).

Circuit of dynamic duty-cycle limiter feedback loop is shown in Fig. 7. Here, we can see the main feedback loop PID controller (can be also be part of the current-mode controller), and the dynamic duty-cycle limitation circuit connected to the detection circuit from Fig. 5. The dynamic limitation circuit interacts with the PID controller via programmable saturation block. In order to protect the high-impedance voltages \(V_{\text{1-(D AVG)}}\) and \(V_{\text{D AVG}}\), the duty-cycle limitation controller is realized by an OTA with very high input impedance [7]. The voltage buffer creates a low-impedance output with small derivative response, which allows to improve the speed of the duty-cycle limitation feedback loop.

The block of programmable saturation shown in Fig. 7 is placed inside main PID controller. This allows to prevent the integrator from accumulating an input error, when the main feedback loop is saturated (anti wind-up [8]). In fact, programmable saturation block is realized by powering the last (output) stage of the PID operational amplifier by \(V_{\text{ERROR MAX}}\).

Operation of the dynamic duty-cycle limitation can be demonstrated by the load transient simulation shown in Fig. 8. Here, before applying a \(6\Omega\) load, converter operates in regulation, \(V_{\text{1-(D AVG)}} > V_{\text{D AVG}}\) and \(V_{\text{ERROR MAX}}\) is clamped to \(V_{\text{OUT}}\). By applying \(R_{\text{LOAD}} = 6\Omega\), output voltage starts dropping below desired value, \(V_{\text{1-(D AVG)}}\) and \(V_{\text{D AVG}}\) approach, and PID output \(I_{\text{ERROR}}\) tries to compensate decreasing \(V_{\text{OUT}}\). Simultaneously, \(V_{\text{ERROR MAX}}\) decreases with \(V_{\text{OUT}}\), until \(V_{\text{1-(D AVG)}}\) crosses \(V_{\text{D AVG}}\). At this time, \(V_{\text{ERROR MAX}}\) falls below \(V_{\text{OUT}}\), and clamps the value of \(V_{\text{ERROR}}\). Now, regulation of the converter output voltage is provided by the dynamic duty-cycle limiter at \(D = D_{\text{CRIT}}\,\text{and } V_{\text{1-(D AVG)}} = V_{\text{D AVG}}\). As we can see, the converter output voltage \(V_{\text{OUT}}\) reaches highest possible value, and allows to deliver maximal output power (voltage) for given operating conditions. This is visualized in Fig. 8 by comparison with open-loop simulation of the converter with \(6\Omega\) load, and \(D\) linearly increasing from zero to one.
IV. INPUT SOURCE RESISTANCE POWER SENSING

As given by the power balance condition (5), the power dissipated in converter must be equal to the power dissipated by the load. However, if the input source resistance $R_{IN}$ is not negligible, it must be included in the consideration ($R_{IN}$ and $R_{COIL}$ are serially connected). In other word, power $R_{IN}I_{COIL}^2$ is to be added to $P_{LOSS}$ of (5). This situation is shown in Fig. 9.

The difficulty of the input source resistance power sensing can occurs e.g. in the battery-powered converter, or converter powered by the photovoltaic cell (without MPTT – maximum power point tracking feature), where $V_{IN(0)}$ is not available.

A solution to bypass the input power sensing problem is to emulate the input source voltage $V_{IN(0)}$ and refers the inductor RC filter resistance $R_1$ to this voltage. This configuration is shown in Fig. 10. Here, an estimation of the input voltage $V_{IN(0)}$ is provided. This estimation is based on the generation of estimated voltage $V_{IN\_EST}$. If the estimated $V_{IN\_EST}$ is accurate enough, RC filter $R_1C_1$ measure the average voltage on the serial connection of $R_{IN}$ and $R_{COIL}$.

REFERENCES


