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Ph.D. Dissertation

**ADVANCED FPGA-BASED READOUT
ELECTRONICS FOR STRIP DETECTORS**

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Anotace

V posledních letech se polovodičové detektory ukázaly jako vynikající nástroje pro měření ionizujícího záření. Hybridní pixelové detektory, nejnovější vývojový stupeň polovodičových detektorů, vzhledem k jejich vysokým nákladům na plochu a typicky malé jednotkové velikosti, nejsou obvykle používány pro aplikace ve velkém měřítku. Zde stripové detektory, technologie před pixely, poskytují levnější způsob sledování, počítání částic, a s poslední generací ASIC čipů také spektroskopii a časová měření. Další výhodou je, že front-end ASIC je umístěn vedle senzoru, kde může být snadno chráněn před primárním ozářením. Obvykle také neexistuje žádný přenos tepla mezi senzorem a ASIC a v případě poškození lze senzor nebo ASIC jednoduše vyměnit.

Cílem této práce bylo zkoumat schopnosti stripových detektorů jako spektroskopů měření tradičních zdrojů ionizujících částic, jako jsou fotony nebo alfa-částice, které mají dobře definovanou energii. K tomuto účelu byl vyvinut 128 stripový nízko šumový měřicí systém založený na FPGA, společně s potřebným programovým vybavením, připojený ke křemíkovému stripovému detektoru.

Kromě toho byly vyvinuty adekvátní metody vyrovnání různých hladin šumu a kalibrace tak, aby se dosáhlo rovnoměrnější odezvy z kanálů a tím i lepšího rozlišení energie. Aby bylo možné číst všech 128 kanálů použitého snímače, musely být použity 4 nezávislé ASIC čipy, z nichž každý obsahoval 32 kanálů.

V průběhu měření bylo získáno σ 1.6 keV pro průměr všech kanálů v energetickém rozsahu 15-60 keV, které překonaly srovnatelné Si hybridní pixelové detektory typicky mající σ 2.3 keV [1]. Pomocí 6-sigma vzdálenosti k elektronické hladině šumu bylo stále dosaženo systémové prahové úrovně 3 keV.

Tento výzkum poskytuje cenné informace pro více aplikací, ve kterých by mohly být stripové detektory efektivně použity jako náhrada hybridních pixelových detektorů.

Klíčová slova

Ionizující záření, dioda s opačným biasem, pár elektron-díra, stripový detektor, vyčítací elektronika, tvarovací čas, spektroskopie, ASIC, FPGA, VHDL.

Abstract

In recent years semiconductor detectors have proven to be excellent tools to measure ionizing radiation. Hybrid pixel detectors, latest development stage of semiconductor detectors, due to their high cost per area and the typically small unit size, are usually not employed for large scale applications. Here strip detectors, technology before pixel, provide a cheaper way of particle tracking, counting, and with the latest generation of ASICs also spectroscopy and timing. Additional advantage is that the front-end ASIC by design is located next to the sensor, where it can be shielded from primary irradiation easily. Also there is typically no mentionable heat transfer between sensor and ASIC and, in case of damage, the sensor or ASICs can simply be exchanged.

The aim of this thesis was to investigate the performance of strip detectors as spectroscopes by measuring typical sources of ionizing particles, such as photons or alpha-particles, having a well-defined energy. To this end a 128-strip low noise FPGA-based readout system was fabricated alongside a corresponding dedicated software tool and connected to a Si strip sensor.

In addition, adequate equalization and calibration methods were developed in order to get a more uniform response from the channels and hence better energy resolution. In order to read all 128 channels of the sensor employed, 4 independent readout ASICs, featuring 32 channels each, had to be used.

In the current investigation a sigma of 1.6 keV was obtained for the mean of all channels within the energy range of 15-60 keV, outperforming comparable Si hybrid-pixel detectors typically having a sigma of 2.3 keV [1]. Using a 6-sigma distance to the electronic noise level it was still obtained a system threshold level of 3 keV.

This research provides valuable information for multiple applications in which strip detectors could be used efficiently to replace hybrid-pixel detectors.

Key words

Ionizing radiation, reversed-biased diode, electron-hole pair, strip detector, readout electronics, shaping time, spectroscopy, ASIC, FPGA, VHDL.

Declaration

I hereby submit this work, written during my studies at UWB in Pilsen, for review and advanced defence. I confirm that this is my own work and all used literature and sources are cited and listed in this document. Only legal and licensed software was used.

In Pilsen

.....

Glossary

List of Symbols

n	n-type semiconductor
p	p-type semiconductor
n ⁺	highly doped n-type semiconductor
p ⁺	highly doped p-type semiconductor
μ_n	Electron mobility
μ_p	Hole mobility
γ	Gamma
τ	Time constant Tau
Ω	Ohm
Si	Silicon
Ge	Germanium
Cd	Cadmium
Te	Tellurium
Ga	Gallium
As	Arsenic
Sb	Antimony
K	Potassium
Cs	Caesium
Zr	Zirconium
Mo	Molybdenum
In	Indium
Cu	Copper
Am	Americium
Pu	Plutonium
Cm	Curium
Pb	Lead

List of Abbreviations

R	Resistance
C	Capacitance
Q	Charge
t	Time
V	Volt
s	Second
PM	Photomultiplier
aC	atto-Coulomb
fC	femto-Coulomb
keV	kilo-electron Volt
LPF	Low Pass Filter
HPF	High Pass Filter
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
CPLD	Complex Programmable Logic Device
ASIC	Application-Specific Integrated Circuit
SMA	Sub Miniature version A
HSMC	High Speed Mezzanine Card
FPGA	Field Programmable Gate Array
FSR	Fast Shift Register
FTDI	Future Technology Devices International Ltd.
FWHM	Full Width at Half Maximum
GUI	Graphical User Interface
LVDS	Low-Voltage differential signaling
PCB	Printed Circuit Board
USB	Universal Serial Bus
VHDL	VHSIC Hardware Description Language
RW	Read Write
EN	Enable
CK	Clock
CS	Chip Select

FL	Flag
SDI	Serial Data Input
MUX	Multiplexer
TRIM	Trimming
CERN	Conseil Européen pour la Recherche Nucléaire
BNL	Brookhaven National Laboratory
IEAP	Institute of Experimental and Applied Physics
CTU	Czech Technical University in Prague
SINTEF	Stiftelsen for industriell og teknisk forskning
ENC	Equivalent Noise Charge

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Introduction

Semiconductor radiation detectors have benefited from the fast evolution of micro-electronics and materials science in semiconductor processing. High integration of transistors and hence functionalities can be achieved in readout ASICs as well as very good sensor quality for different materials, something that was simply impossible in the past. As a result of that, semiconductor detectors have been increasingly used in the most important particle physics laboratories around the world, providing clear advantages compared to other common detector types [2], [3]; energy resolution, precise position measurement, low noise, low power, high readout speed, availability of signals in electronic form and minimum material make semiconductor detectors an ideal solution in a vast number of applications. At the same time, other fields of science and technology as nuclear physics, optical and X-ray astronomy, medicine and material testing have benefited as well [4], [5].

Several types of semiconductor detector exist, each one offering particular advantages. Among them, pixel and strip detectors are the most commonly used. Currently, pixel detectors are the prevalent choice due to their good resolution, fast performance, 2D reconstruction of events, and production of unambiguous hits; however, they possess disadvantages which also limit the number of potential applications: small sensing area, interaction of readout ASIC with radiation, prominent heat transfer from the readout chip to the sensor when not operated under cooling, high precision and complex bump-bonding process required to connect the sensor and the readout ASIC, making the device very expensive.

Strip detectors have been mainly used as tracking devices, proving to be a very good option for position-sense and counting of particles. Nevertheless, thanks to new generations of ASICs available nowadays for strip sensors it is possible, as in the case of pixel detectors, to get complementary information about the particles interacting with the sensor, for example, time of arrival or energy. Given the previously mentioned limitations associated to pixel detectors, strip detectors arise as an alternative way of measuring ionizing radiation, providing good energy resolution, position-sensing, possibility of isolation of the readout ASIC from radiation, bigger size and different shapes, and affordable price; this is especially important in applications where covering big areas is imperative and where price of using pixel detectors constitute a strong limitation.

Since the capabilities of strip detectors for tracking are well known, studied and tested, this thesis aims to evaluate the scope of strip detectors for spectroscopy and as a potential replacement of pixel detectors for certain applications which will be well benefited from their features. To accomplish this task, 128-strip low noise FPGA-based strip sensor readout systems were fabricated, and custom equalization and calibration processes to improve the results were designed and tested. Afterwards, the results were compared with a well-known pixel detector (Timepix).

This thesis starts by providing a review of the most common methods and types of detectors used to measure ionizing radiation. Then a deeper analysis of the strip detectors and their applications is discussed. Later on, an overlook of the strip-based systems developed in this thesis is provided, including GUI software and firmware details. Subsequently, the methods

of equalization and calibration developed specifically for these systems are discussed. Finally, results, analysis and conclusions are provided.

1 Detectors of Ionizing Radiation

1.1 Gas Filled Detectors

The principle of operation of Gas Filled Detectors is based on the fact that the radiation passing through a gas can ionize the gas molecules and then produce charge pairs. Using an external electric field the charge pairs can be moved in opposite directions toward the electrodes (positive and negative). As a result, the charges moving generate an electric pulse containing information about the detected radiation that can be measured by the appropriate electronics [6].

The high voltage applied to the electrodes depends on the design and mode of operation of the detector, and can range from less than 100 volts to a few thousand volts.

Charge pairs moving in the gas perturb the external electric field and produce a pulse at the electrodes. The measurement of that pulse gives information about the energy of the radiation and/or its intensity. As in any kind of detector, an appropriate calibration is necessary before the measurement starts to obtain real and precise information [6].

The geometry of the detector, the gas and the high voltage applied to the electrodes controls the production of the charge pairs and their kinematic behaviour in the gas [6].

1.1.1 Ionization Chambers

From all the Gas Filled Detectors, the Ion Chambers (Figure 1) are the simplest and most widely used. The term ionization chamber has been used for the type of detectors using as principle of operation the collection of ion pairs from gases [7].

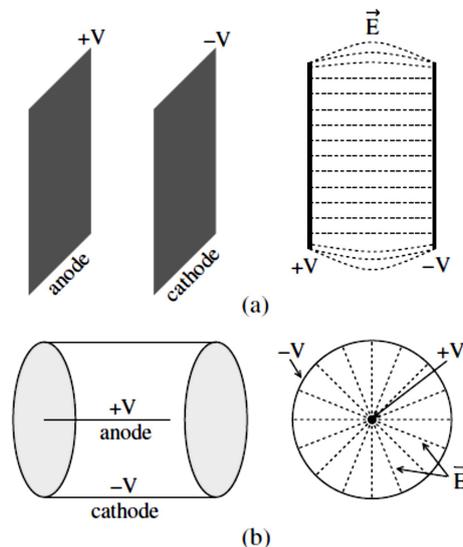


Figure 1. (a) Parallel plate ion chamber and its electric field in the active volume. (b) Cylindrical ion chamber and its electric field in the active volume [6].

When a fast charged particle passes through the gas contained in the chamber, it creates both excited molecules and ionized molecules along its path. The term ion pair refers specifically to a positive ion and a free electron generated after a neutral molecule is ionized [7].

Because of their simple design and well known physical processes, ionization chambers have been widely used to measure certain types of radiation: X-rays, beta particles and gamma rays [6].

1.2 Liquid Filled Detectors

The principle of operation of Liquid Filled Detectors is similar as for Gas Filled Detectors: The incident radiation creates a charge pair in the liquid under the effect of an electric field that generates a change in current or voltage measurable at the electrodes. Nevertheless, in liquids the energy needed to create a charge pair doesn't depend on the type of liquid as it happens in gases, but, since the energy states in liquid state are quite different from those in gaseous state the process of charge pair production is more complicated in liquids [6].

Among the benefits of using liquids instead of gases are the possibility of obtaining more charge pairs for the same amount of energy deposited, and higher total deposited energy per unit path due to their higher molecular density, however, higher density means higher spatial proximity of molecules which increases the recombination probability of charges. This is a drawback for the detectors since it introduces uncertainties in the proportionality of measured pulse height with the deposited energy [6]. It is important to mention that the operation of liquid-noble-gas ionisation chambers requires cryogenic equipment. This technical disadvantage can be overcome by the use of 'warm' liquids. The problems associated with flammability and toxicity can be handled if the liquids are sealed in vacuum-tight containers. These 'warm' liquids show excellent radiation hardness [8].

A good example of the use of Liquid Filled Detectors is the calorimeters, commonly used in high energy physics experiments. There it is used liquefied argon as mean of detection in large area detectors. As the density in liquids is 1000 times higher than in gases, the energy absorption is 1000 times higher, which means they are an excellent mean of detection for relativistic particles and the photon-detection efficiency increases by the same factor [6], [8].

Liquid Filled Detectors can be used as scintillation detectors using liquid xenon to produce light when its molecules are excited by the incident radiation [6].

The Liquid Filled detectors have two characteristics that make them suitable for dosimetry and radiation therapy: they are more radiation tolerant than semiconductor detectors and they have smaller size than gas filled detectors. For high radiation fields they offer good precision and can even be designed to provide a good degree of spatial resolution [6].

1.3 Scintillation Detectors and Photodetectors

The conversion of the energy deposited by a particle going through a scintillation material into electrical signals is done in an indirect way. There are two basic steps necessary to accomplish that task: The first step, done in the scintillation material, consists of converting

the energy deposited into visible light [8]. Here the process is very simple: when the atoms of incident radiation interact with the atoms of the scintillation material, they transfer part of their energy to the atoms, exciting them and going into short lived excited states. Then, when they return to their stable states they emit photons mostly in visible and ultraviolet regions of the spectrum [6]. The second step consists of transferring of the visible light either directly or via a light guide to an optical receiver (photomultiplier, photodiode, etc.) [8], as shown in figure 2.

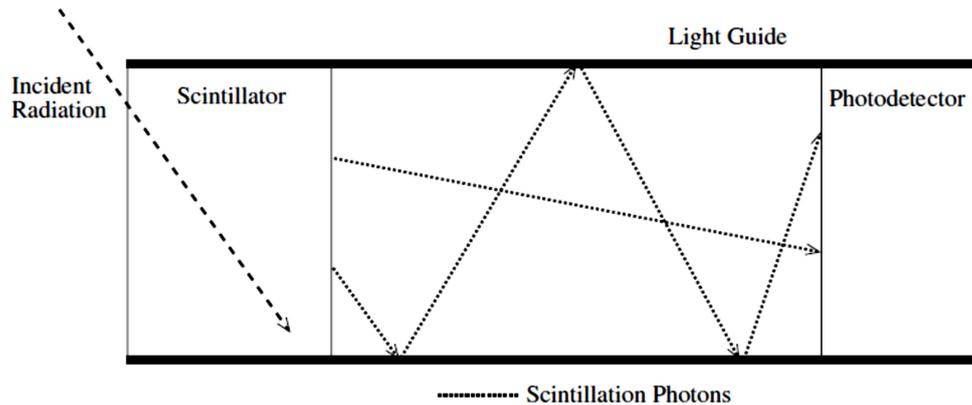


Figure 2. Transmission of scintillation photons by reflection through a light guide to reach a photodetector [6].

The indirect detection mechanism has the disadvantage of need a much more larger energy to produce one photoelectron (50 eV for the best scintillation counters) compared to the energy necessary to produce an electron-hole pair in solid-state ionization detectors (3.65 eV). However, this drawback is compensated by the possibility to build cheap large size and mass detectors using scintillation materials [8].

Although the efficiency of a typical scintillation material to emit photons after the interaction with ionizing radiation is relatively low (10% to 15%), implying that a high percentage of the scintillation photons are wasted away, it is still possible to develop a highly efficient radiation detector. This is accomplished during the second step using a photon detector that has high photon collection and counting efficiency. However, when the scintillation detectors are used in low field environment this is still one of the most problematic things, even using the more efficient photocathode materials that have been developed recently. Additionally, it is well known that the optical properties of the scintillators are vulnerable to atmospheric conditions as moisture or temperature fluctuations. Similarly, changes in pressure may cause cracks. Due to this fact, the mechanical stability of solid scintillators is a major concern for detection systems [6].

The scintillators can be classified as organic and inorganic. Organic scintillators are extensively used in radiation detectors. They can be found in liquid, solid or gaseous states. The main advantage of organic scintillators is the flexibility to be produced in virtually any geometry. Inorganic scintillators have usually crystalline structures. These materials are generally denser and have higher atomic number than organic scintillators. This makes them very attractive when it is needed high stopping power. Another advantage is their higher light output compared to organic scintillators [6].

The most commonly used photon detector is the photomultiplier (PM). The light in the range from visible to ultraviolet liberates electrons from a photocathode due to photoelectric effect. Photomultipliers with semi-transparent photocathode are commonly used. This photocathode is a very thin layer of a semiconductor compound (SbCs, SbKCs, etc.) deposited to the interior surface of the transparent input window [8].

The basic concept behind a photomultiplier involves the conversion photon coming from the scintillation into an electron and then the multiplication of this electron into a very large number of electrons. As it was mentioned before, the photon-electron conversion takes place in a thin material called photocathode. The electrons produced in the photocathode are accelerated towards a metallic structure called dynode which releases a large number of electrons due to the impact. The new secondary electrons are then accelerated towards another dynode, which also multiplies their number. The process is repeated several times by letting the electrons pass through a series of dynodes. At the end of the chain of amplification it is generated an output pulse with amplitude large enough to be easily measured by the associated electronics [6], as shown in figure 3.

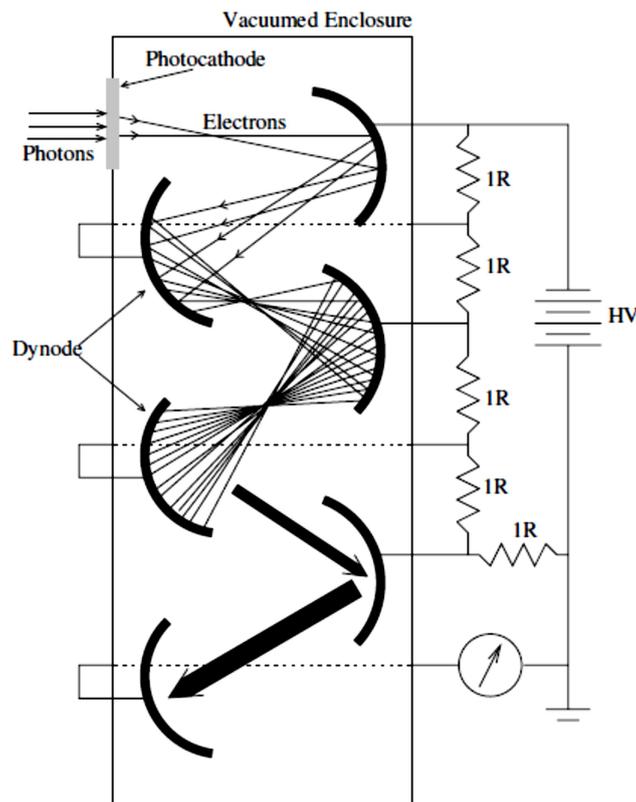


Figure 3. Working principle of a typical side-on type PMT. The amplified signal is measured at the final dynode or anode [6].

Another commonly used type of detector is called photodiode, and the same as photomultipliers, can be used to detect photons produced by scintillation materials. A

photodiode is made of a semiconductor material that has been appropriately doped, but in this case it produces electron-hole pairs instead of just electrons as in the case of photomultipliers. The efficiency of a photodiode can be as high as 80%, which certainly solves the problem of photomultipliers when used in low level radiation environments [6].

When the measurements are carried out in extremely low radiation fields, there is another special kind of photodiode detector, called the avalanche photodiode. In a photodiode the electron-hole pairs produced by the incident radiation are multiplied through an avalanche process. This multiplication is similar to that of electrons in photomultipliers but with the advantage that there are no mechanical structures involved. The result of the electron hole multiplication is the transformation of a very low level signal into a pulse large enough to be measured by the electronics [6].

A photodiode consist of a very thin layer of highly doped p+ silicon covered on the top by a silicon oxide film, a layer of moderately doped n silicon called '*i layer*', and ending with a highly doped n+ silicon layer. The structure is attached to a ceramic substrate and covered with a transparent window [8], as shown in figure 4.

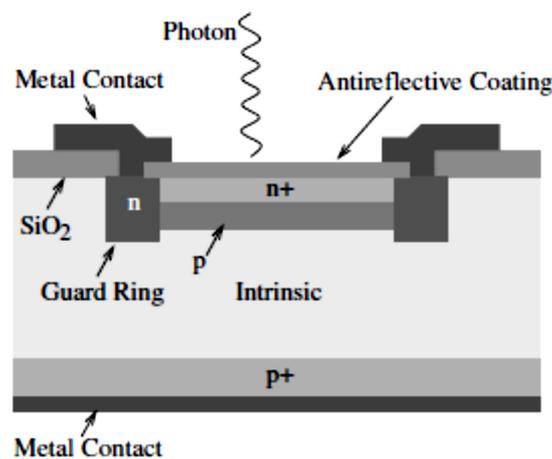


Figure 4. Typical structure of a silicon based reach-through type avalanche photodiode [6].

A bias voltage is applied to the n silicon layer or '*i-layer*' to deplete the diode. Then, when a photon enters the depletion area, it goes through the '*i-layer*' and creates an electron-hole pair that is separated by the electric field which exists in this area due to the bias voltage effect. The photodiode signal is usually read out by a charge-sensitive preamplifier followed by a shaping amplifier with optimal filtering [8].

1.4 Semiconductor Detectors

1.4.1 Reverse-Biased Diode

A diode consists of a highly doped p^+ region in contact with a very lowly doped n substrate. The back of the substrate is in contact with a highly doped n^+ layer. The purpose of the n^+ layer is to provide a good ohmic contact from the aluminium to the substrate and to allow the operation of the device in over depleted mode [4].

In the field of radiation detection, reverse-biased diode is a very important part. The reversed-bias diode acts as a capacitor where the undepleted p and n regions are the electrodes and the depletion region is the dielectric due to its devoid of mobile carriers. The electric field in the depletion region moves mobile carriers to the electrodes, forming a kind of ionization chamber, as shown in figure 5. The depletion region formed by thermal diffusion is thin, in order of micrometres; however the width of the depletion region can be increased by applying a reverse bias voltage [5]. Increasing the reverse bias voltage increases the width of the depletion region and therefore the sensitive detector volume, and simultaneously decreases the detector capacitance [4].

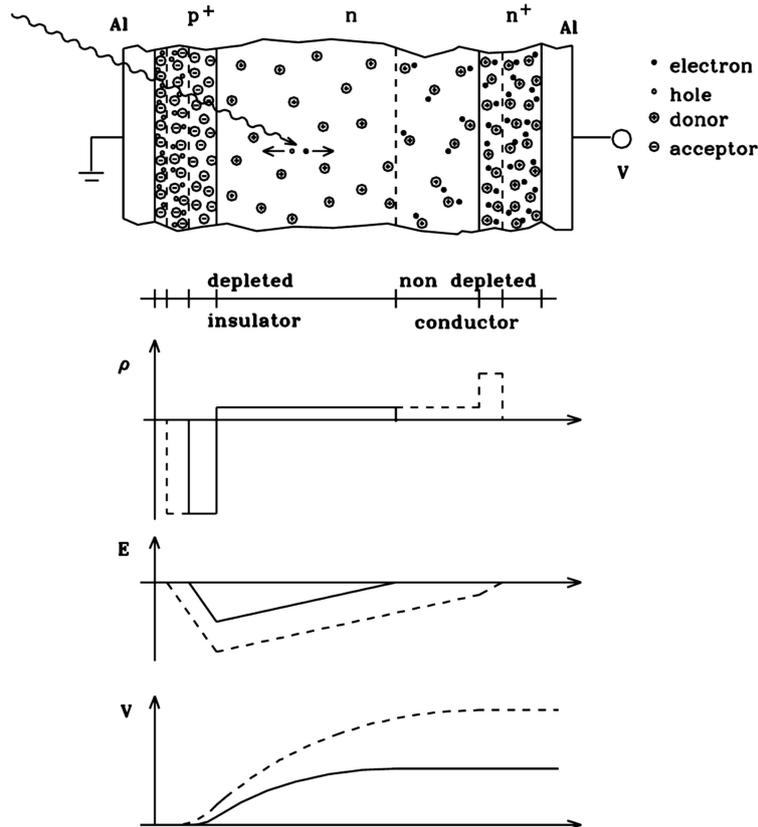


Figure 5. Reverse-biased diode detector: charge density (ρ), electric field (E) and potential (V) for partial (continuous line) and full (dashed line) depletion [4].

This type of detector is used to measure the energy of individual particles, for example in nuclear spectroscopy. The rectifying junctions can be either metal–semiconductor contacts, p–n diode junctions produced by ion implantation or diffusion in the planar technology that now dominates [4].

Semiconductor detectors are used in a large variety of fields in science and technology. These fields include nuclear physics, elementary particle physics, optical and X-ray astronomy, medicine, and materials testing, etc. This encourages the development and constant improving of low-noise low-power readout electronics [4].

Semiconductor detectors are successful due to their unique properties compared to other type of detectors, especially for the detection of ionizing radiation. Examples of these properties are: direct availability of signals in electronic form, extremely precise position measurement, high readout speed, precise energy measurements, and the possibility of integrating detector and readout electronics on a common substrate. As silicon (Si) is the most common material used in the fabrication of transistors and complete microelectronics circuits and also the most common material used in the fabrication of semiconductor detectors, part of the process technology can be easily adapted for the detector production, having an excellent reliability and quality of the products thanks to its highly developed technology [4].

Here there is a comparison of some of the most important semiconductor material properties with the gas filled detectors [4]:

- The small band gap (1.12 eV at room temperature) generates a large number of charge carriers per unit energy loss. Average energy to create an electron-hole pair in Silicon (3.6 eV) is an order of magnitude smaller than in gases (~ 30 eV).
- High density of Silicon (2.33 g/cm³) produces large energy losses in ionizing particles (3.8MeV/cm for a minimum ionizing particle), making it possible to build thin detectors producing good measurable signals.
- Electrons and holes can move almost freely despite of its high material density, then the charge can be rapidly collected (~ 10 ns) and detectors can be used in high-rate environments. (Mobility of electrons $\mu_n = 1450$ cm²/Vs and holes $\mu_p = 450$ cm²/Vs).
- Excellent mechanical rigidity allows self-supporting structures.
- Integration of detectors and electronics is possible in a single device.

The most commonly used semiconductor materials are Silicon and Germanium (Ge), but other compound materials as GaAs and CdTe have been used. The most important difference between silicon and germanium detectors is the factor of two in the band gap and the much shorter radiation length for germanium. Germanium has a high absorption probability that is appropriate for X-ray and almost infrared measurements. However, germanium detectors require cooling [4].

The GaAs material has the advantage of the high mobility of electrons ($\mu_n = 8800$ cm²/Vs), so they are commonly used in ultra-high speed electronics. The interest in GaAs for application in high energy physics has risen due to its high radiation tolerance with respect to reverse bias currents, compared with silicon. However, their used is limited for radiation

detection where large sensitive volumes and a full charge collection are required. The problem of incomplete charge collection is due to trapping by (radiation-induced) defects [4].

1.4.2 Signal Formation

In a detector diode, the depletion width increases with the square root of the reverse bias voltage, meaning that the sensitive volume is increased, but at the same time, the capacitance of the detector is reduced. A higher reverse bias voltage increases the signal charge and reduces the electronic noise when a particle interacts with the detector volume, which is very beneficial. However, the maximum bias voltage that is possible to apply is limited. If this limit is reached or even overpassed, a destructive avalanche effect called '*breakdown*' will appear. At electric fields higher than 105 V/cm the electrons acquire sufficient energy to form secondary electron-hole pairs, which produces the breakdown [5].

On figure 6 it is shown a typical configuration of a detector diode. The detector diodes are usually asymmetrically doped. The bulk material is made of lightly doped n silicon, and forms a junction with a highly doped p⁺ layer. The depletion region is created predominantly into the bulk. The back contact is made of highly doped n⁺ silicon, the same kind as the bulk. This avoids forming a second diode and instead forms an '*ohmic*' contact. Additionally, it can be seen from figure 6 a guard ring which is mean to isolate the wafer edge from the active region. The guard ring is biased at the same potential as the junction contact, so the boundaries of the sensitive volume are the detector electrode and the guard ring. In the gap between the detector electrode and the guard ring, a silicon oxide passivation is usually placed to prevent formation of a conductive path between them [5].

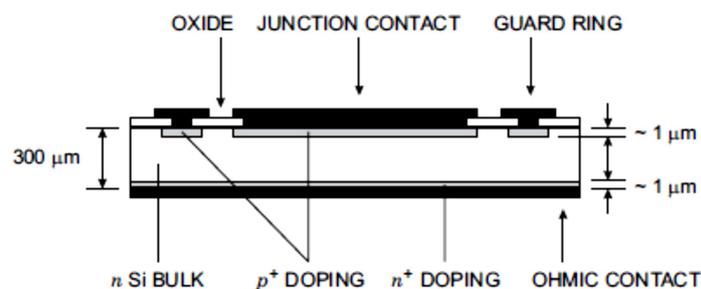


Figure 6. Detector diodes are commonly formed by introducing a highly doped surface layer into a lightly doped bulk. The depletion zone then extends into the bulk. Metallization layers (black) provide electrical contacts to the doped p⁺ and n⁺ layers that form the junction and the back electrode (ohmic contact) [5].

2 Strip Detector-Based Systems

2.1 Strip Detectors

In many applications, it is important not only to know if the detector registered some particles during certain time, but also their position. The best way to accomplish that is to divide a large area diode into many small detectors or subpixels and then to read them out separately. The new small detectors can have strip or pixel shapes and the position is then calculated geometrically using only the subpixels or strips showing signals due to the passage of an ionizing particle [4].

Figure 7 shows the cross section of a strip detector with an n type substrate. There, the strips (highly doped p+ electrodes) are introduced by ion implantation through a mask. The substrate and each strip forms a p-n diode. The gaps between the strips must be controlled to electrically isolate all the adjacent diodes. Then, an aluminium layer is deposited on the strips to provide a low resistance contact to be used by the readout electronics [5].

The precision of strip detectors during a measurement depends mainly on the strip spacing or ‘pitch’ and the readout method. Regarding the ‘pitch’, if this is chosen small enough to have the signal charge collected not only in one but in several strips, the measurement precision can be improved substantially and the point of interaction of a particle can be found by interpolation, e.g. by the centre of gravity of the signal [4].

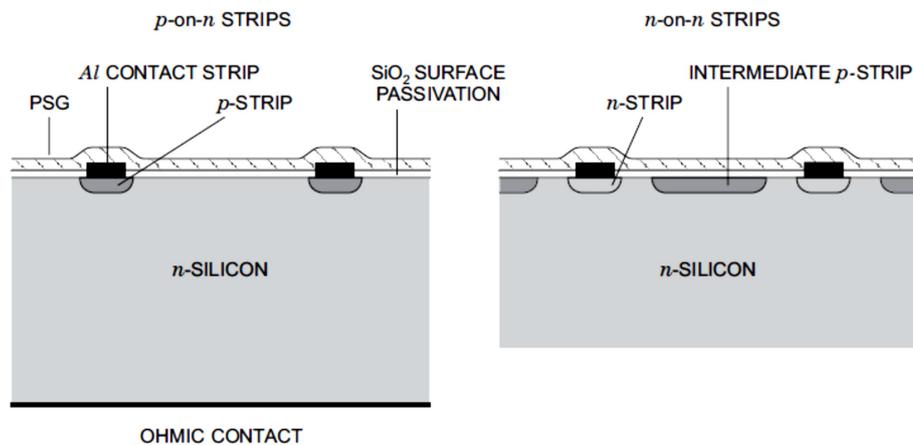


Figure 7. Cross-section of the electrode’s structure in strip detectors. The left shows the junction side of a single-sided detector. In double-sided detectors the electrodes on the ohmic side require additional isolation structures, for example an intermediate p-region as shown at the right. A layer of phosphosilicate glass (PSG) protects the structure [5].

When using strip detectors for tracking or position-sensing of ionizing particles, it is important to highlight that a single strip detector is not enough to have a 2-D coordinate. For that it is necessary to use an arrangement of two single strip sensors, or a double-sided strip sensor.

2.1.1 Double-Sided Strip Detectors

Figure 8 shows a double-sided silicon strip detector. As electrons and holes move in opposite directions due to the electric field produced by the bias voltage, it is feasible to use both types of charge carriers for position measurement by providing charge-collection electrodes on both sides of the wafer [4].

In double-sided strip detectors, the strips on both sides are usually orthogonal to each other, providing a two-dimensional Cartesian coordinate system. However, not in all the cases it is recommended to use right angles between upper and lower strips; it depends basically on the application [6]. Right angles are problematic when used in experiments with high occupancy rates due to the increase of fake or ‘phantom’ events. In order to overcome this situation, a small angle (stereo angle) between upper and lower strips is needed [3]. Even though it is technologically feasible to fabricate double-sided strip detectors having any angle between upper and lower strips, in general the fabrication cost of double-sided strip detectors is higher compared to the fabrication of a pair of single-sided strip detectors, due to extra fabrication processes needed to etch the second wafer side. In that context, if highly penetrating particles are to be tracked, a cheaper solution is to use two single-sided strip detectors and overlap them at the wished angle. In any case, double-sided strip detectors are still much cheaper than pixel detectors.

As it was stated before, the advantage of double-sided strip detectors is that due to the crossed strips of one side respect to the other, projective two-dimensional measurements can be obtained from one single detector. For particles crossing the detector, since the events are produced in both sides of the detector from the same initial charge cloud, a spatial point of interaction similar as for pixel detectors is possible to obtain. For absorbed radiation such as X-rays, two-dimensional measurements become possible. Using analog readouts, it is possible to correlate the signals from both sides to resolve ambiguities when several particles simultaneously hit the detector [4].

On figure 8 it is also possible to see guard rings, placed there to reduce the possibility of electrical break down. It is common to use several guard rings on a detector such that the high voltage gradually decreases instead of a large abrupt change [6].

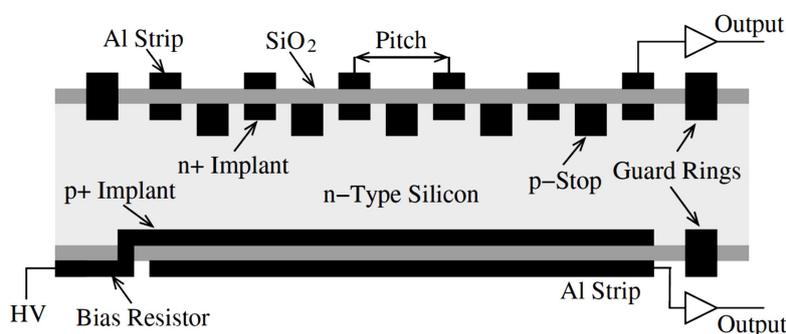


Figure 8. Design of a simple double-sided silicon microstrip detector [6].

2.1.2 AC-Coupled Strip Detectors

There are several advantages of AC coupled detectors compared to DC coupled ones. Probably the main advantage is shielding of the readout electronics from dark current, which can lead to pedestal shifts, a reduction of the dynamic range, and may even drive the electronics into saturation [4].

In order to implement an AC coupled detector, a coupling capacitor has to be added to each channel. External capacitors are not an option due to their big size. In that context, there are two possibilities to solve this situation: one is to include the capacitors inside the readout chips and the second one is to do it inside the sensor. Despite of having the possibility of readout ASICs including the coupling capacitors, it is quite common and simple to implement the capacitors in the sensor.

Figure 9 shows a typical implementation of coupling capacitors in a strip sensor. Here the capacitances are built with a thin silicon oxide layer separating the implantation and metallization of the strips [4].

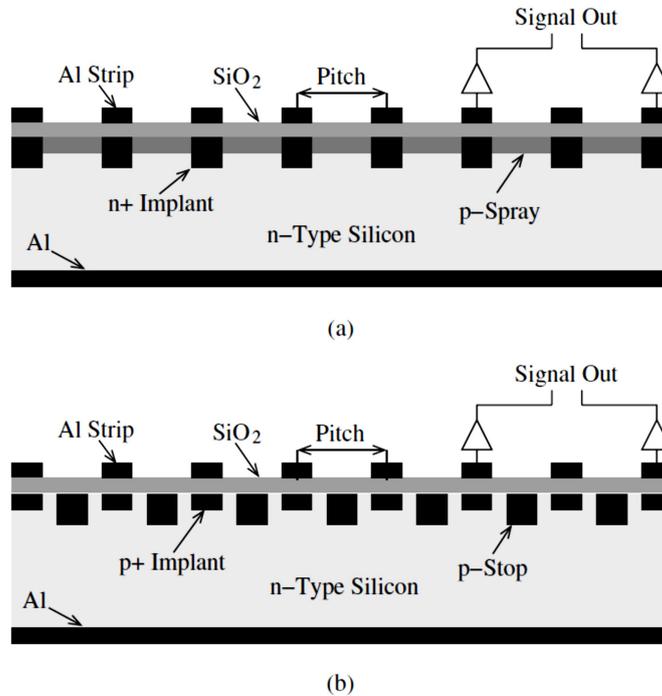


Figure 9. One sided silicon microstrip detector of (a) p-spray and (b) p-stop types [6].

The output signal of each strip is read out through aluminium strips implanted over the n+ strips. Due to the silicon oxide layer, only mirror charges on the aluminium strips are actually seen by the readout circuitry [6].

Additionally, as stated before, to make each strip working properly it is necessary to bias them such that the detector gets fully depleted. Supplying the bias to each strip is not an easy task since it needs to distribute the power through bias resistors attached to the strips. Similarly as for capacitors, the bias resistors take space and must be made as small as

possible. There are several structures used to build the resistors; they include: implanted resistors, polysilicon resistors, and punch-through resistors. Each type has its own pros and cons and the particular choice depends on the type of detector, the radiation environment, and the cost [6].

2.2 Front-End Electronics

All semiconductor systems are composed of the same basic functions. In the case of strip detectors there is no exception, the signal coming from each strip must be amplified and processed for storage and further analysis [5], as shown in figure 10.

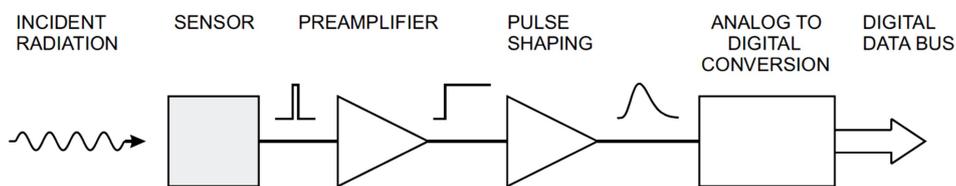


Figure 10. Basic detector functions [8].

Radiation is absorbed in the sensor and converted into an electrical signal. This low-level signal is integrated in a preamplifier, fed to a pulse shaper, and then digitized for subsequent storage and analysis [8], [5]. An important parameter to take into account is the total capacitance in parallel with the input, which is composed by the detector's capacitance and input capacitance of the amplifier. It is a key parameter because the signal-to-noise ratio increases when the total capacitance decreases [8].

Here a description of the basic stages of a readout system is provided:

2.2.1 Sensor

The sensor converts the energy deposited by a particle to an electrical signal. As it was explained in the previous sections, this takes place when the energy is absorbed in a semiconductor, which produces mobile charge carriers (electron-hole pairs). The electric field created in the sensor by the application of a high voltage bias supply sweeps the charge carriers to electrodes, inducing an electrical current. The number of electron-hole pairs is proportional to the energy deposited by the particle in the semiconductor material, and integrating the current signal it is possible to obtain the corresponding charge, which is proportional to the energy [5].

2.2.2 Preamplifier

The signal charge produce by the sensor is quite small, about 50 aC for 1 keV X-rays and 4 fC in a typical high-energy tracking detector, so the sensor signal must be amplified. The magnitude of the signal produced by the sensor is affected by statistical fluctuations, and

electronic noise that degrades the signal integrity. In this case it is very important to carefully design the sensor and preamplifier to minimize the electronic noise. Equally, the contribution of electronic noise also relies on the next stage, the pulse shaper [5].

2.2.3 Pulse Shaper

The main function of pulse shapers in semiconductor detector systems is to improve the signal-to-noise ratio. Although the signal from the sensor is a pulse, the signal power is also distributed in frequency space, quantified by the pulse's Fourier transform. As the frequency spectra of the signal and the noise are different, it is feasible to improve the signal to noise ratio through a filter that attenuates the noise and leave the signal. However, changing the frequency response also changes the time response, the pulse shape, so this function is called pulse shaping. At the same time, improving the signal-to-noise ratio commonly implies reducing the bandwidth, which increases the duration of the pulse, as shown in figure 11 [5].

The pulse shaper determines the bandwidth of the system and hence the overall electronic noise contribution. The shaper also has the important task of limiting the duration of the pulse, which sets the maximum signal rate that can be allowed [8].

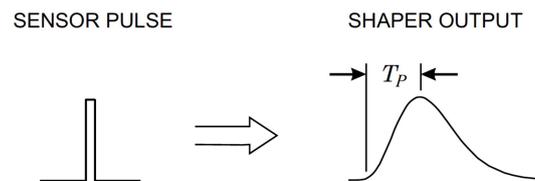


Figure 11. In energy measurements a pulse processor typically transforms a short sensor current pulse to a broader pulse with a peaking time T_p [5].

As we are not interested into measure just one pulse but a series of pulses, usually happening at a high rate, it is important to carefully define the shape of the pulses to be used. If the width of the pulses is too large, it will lead to pile-up of successive pulses, as shown in Figure 12 (left), and the system measuring the peak amplitude will give an erroneous result for the second pulse. The Pile-up can be decrease by reducing the pulse width, as shown in Figure 12 (right) [5].

Figure 13 shows how the transformation process of the pulse shown in Figure 11 is done. The preamplifier is configured as an integrator, and converts the narrow current pulse coming from the sensor into a step impulse with a long decay time. Then it is shown the shaper as a combination of a high pass filter (HPF) and a low pass filter (LPF). The CR high-pass filter introduces the desired decay time and the RC low-pass filter limits the bandwidth and sets the rise time. Although pulse shapers are in reality much more complicated than a simple CR-RC shaper, the CR-RC shaper shown in figure 13 contains the essential features of all pulse shapers, a lower frequency bound and an upper frequency bound [5].

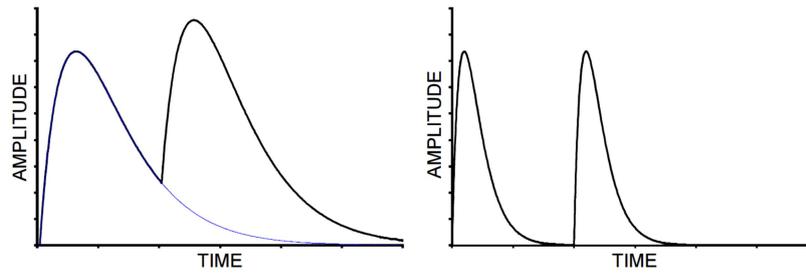


Figure 12. Amplitude pile-up occurs when two pulses overlap (left). Reducing the shaping time allows the first pulse to return to the baseline before the second pulse arrives [5].

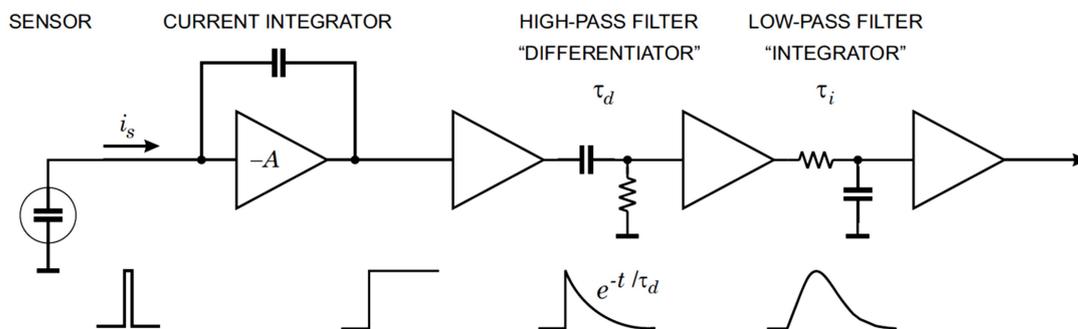


Figure 13. Components of a pulse shaping system. The current signal from the sensor is integrated to form a step impulse with a long decay. A subsequent high-pass filter (“differentiator”) limits the pulse width and the low-pass filter (“integrator”) increases the rise-time to form a pulse with a smooth cusp [5].

The shaper feeds an analogue to digital converter ADC, which converts the magnitude of the analogue signal into a digital data word ready to be stored and processed. When the pulse shape doesn’t change but only the peak amplitude, the height of pulse is equivalent to the signal charge. This kind of measurement is called ‘*pulse-height*’ analysis [8].

Noise and speed are two important features that the design of a system must really take into account. An ideal system would have a reduced noise and an increased speed, but these two features are mutually opposed. In that case it is necessary to find a compromise between them. As it depends on the application, sometimes it is crucial to have low noise or sometimes it is more important to have a good rate capability. Usually a compromise between the two must be found [5].

2.2.4 Digitizer

The last step in the basic stages of a readout system is the analog to digital conversion. The analog to digital conversion transforms a set of pulse amplitudes to discrete steps, each corresponding to a unique output bit pattern. An example of a simple ADC is shown in figure

14. In this case, the analog signal is fed in parallel to a bank of comparators with monotonically increasing thresholds, provided by a resistor voltage divider. Although this technique is very fast, it requires many comparators, as the number of comparators determines the resolution [5].

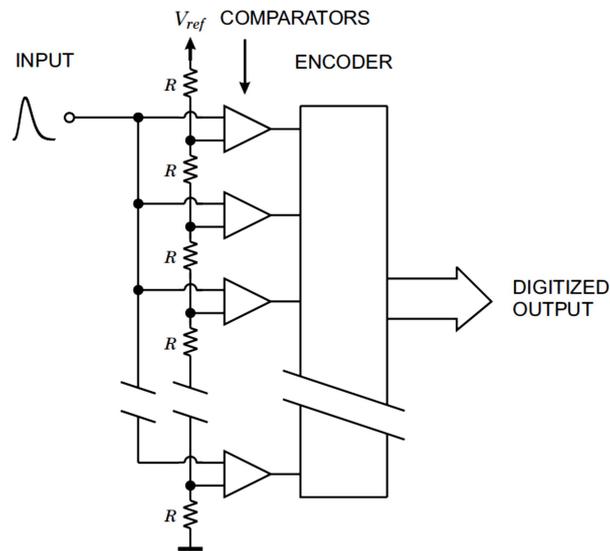


Figure 14. A conceptually simple technique for analog-to-digital conversion utilizes a bank of comparators with increasing threshold levels. The address of the highest level comparator responding to a signal is encoded to provide a binary output [5].

A similar situation as with the pulse shaper occurs here. There must be a compromise between the features of the device according to the application. In this particular case, the speed of conversion of the ADC is an important characteristic. However, when the speed is increased the power dissipation increases too, which is very problematic for some power sensitive applications. On the other hand, speed and resolution are opposing parameters and there must be a trade-off according to the application [5].

3 Radiation Spectroscopy

Radiation spectroscopy refers to techniques using different properties of radiation to study materials and particles. It is well established its usefulness in research and industrial environments. The biggest advantage of radiation spectroscopy lies in the fact that this is a non-destructive technique. Thanks to its direct industrial applications and research value, there has been an immense development of instrumentation and techniques [6].

When the aim of a radiation detector is to measure the energy distribution of the incident radiation, it can be referred to as the general term '*radiation spectroscopy*'. One important property of detectors in radiation spectroscopy is its response to a source of mono-energetic radiation. Figure 15 shows a differential pulse height distribution produced by a detector exposed to this kind of radiation. This distribution is called the '*response function of the detector*' [7].

It is also possible to see on figure 15 two curves representing the same number of pulses, which implies that the areas under both peaks are equal. The curve named '*good resolution*' shows one possible distribution of a good detector around an average pulse height H_0 . On the other hand, the curve named '*poor resolution*' shows the response of a detector with inferior performance [7].

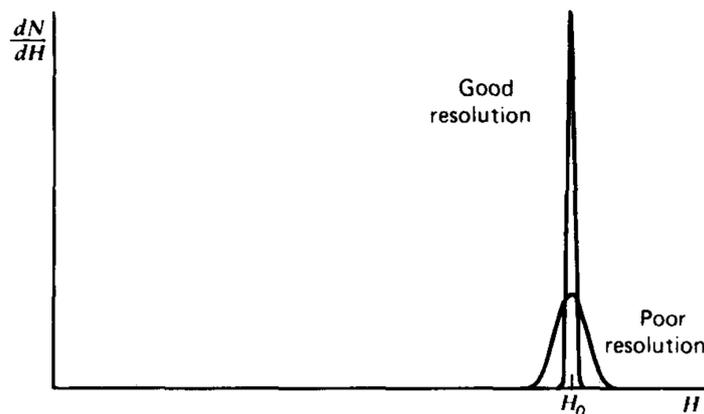


Figure 15. Example of response functions for detectors with relatively good and relatively poor resolution [7].

Even though both curves are centred at the same average value H_0 , the width of the distribution in the poor resolution curve is much greater. This broad distribution shows that even if the same amount of energy is deposited in the detector during each event, there is a large amount of fluctuations from pulse to pulse. If the fluctuations are made smaller, the width of the peak will be smaller too and it will approach a sharp spike similar to a mathematical delta function [7].

3.1 Energy Resolution

Figure 16 shows the formal definition of detector energy resolution.

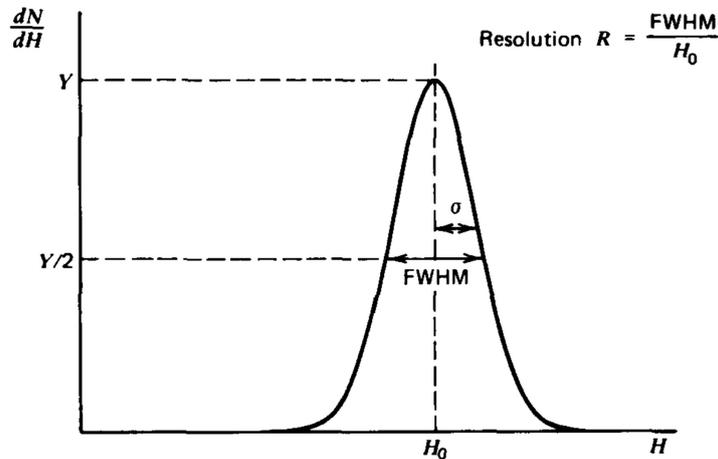


Figure 16. Definition of detector resolution. For peaks whose shape is Gaussian with standard deviation σ , the FWHM is given by 2.35σ [7].

To obtain the differential pulse height distribution it is necessary the assumption that only radiation for a single energy is being recorded. The full width at half maximum (FWHM) is illustrated in the figure 16 and it is defined as the width of the distribution curve at a level that it is half of the maximum amplitude of the peak. The energy resolution of a detector is defined as the FWHM divided by the location of the peak centroid H_0 . Then, the energy resolution R is a dimensionless fraction, usually shown as a percentage. For example, the semiconductor diode detectors used in alpha spectroscopy can have an energy resolution less than 1%. Scintillation detectors used in gamma-ray spectroscopy normally show an energy resolution in the range of 5-10%. It is important to mention that if the energy resolution is smaller, the possibility to distinguish between two radiations whose energies lie near each other is higher. An approximate rule of thumb states that peaks are identifiable when their energies are separated by more than one value of the detector's FWHM [7].

There are several sources of fluctuation in the response of detectors that degrade the energy resolution. These include any drift of the operating characteristics of the detector during the measurements, sources of random noise in the detector and in the instrumentation system, and statistical noise of the measured signal itself. The statistical noise represents an irreducible minimum amount of fluctuation that will be present in the detector signal no matter how perfect the other parts of the system are made. Since the statistical noise represents the dominant source of fluctuation in many detector applications, this is considered as an important limit on the detector performance [7].

3.2 Applications of Strip Detectors

3.2.1 High-Rate X-Ray Spectroscopy

In X-ray spectroscopy, the strip detectors are not used in their usual role of providing position sensing but as a tool to measure the energy of incoming particles, and achieving high rates by distributing the total rate over many parallel readout channels. In the case of localized charge deposition (γ -gamma and X-rays of < 30 keV in silicon), where the energy deposition is dominated by photoelectric absorption, if a sensor electrode is segmented N times, the rate in a single electrode is $1/N$ of the total. Additionally, the segmentation of the sensor area reduces the capacitance per electrode, providing the possibility to achieve the same noise level at a smaller shaping time, and this increases the rate capability [5].

Figure 17 shows results of the noise vs. peaking time in a strip detector. The lower three curves (left) show decrease of the noise level when increasing the peaking time. At the same time, the lower capacitance generates lower noise. When using small peaking times the noise is dominated by the white voltage noise component, so it decreases with peaking time. At larger peaking times the noise is dominated by the $1/f$ component, whose contribution is independent of peaking time [5].

Additionally, the strip sensor introduces the shot noise from the reverse bias current. This noise increases at larger peaking times (round solid dots in figure 17). As the bias current is strongly dependent on temperature, cooling of the sensor becomes important in order to reduce it, as shown in figure 17 (filled square symbols). When optimizing the detector and the preamplifier to reduce the white and $1/f$ noise, the result is as shown in the graphic on the right on figure 17. Here the current noise from the sensor is negligible because of cooling, and the 'flat' noise vs. peaking time indicates that $1/f$ noise dominates [5].

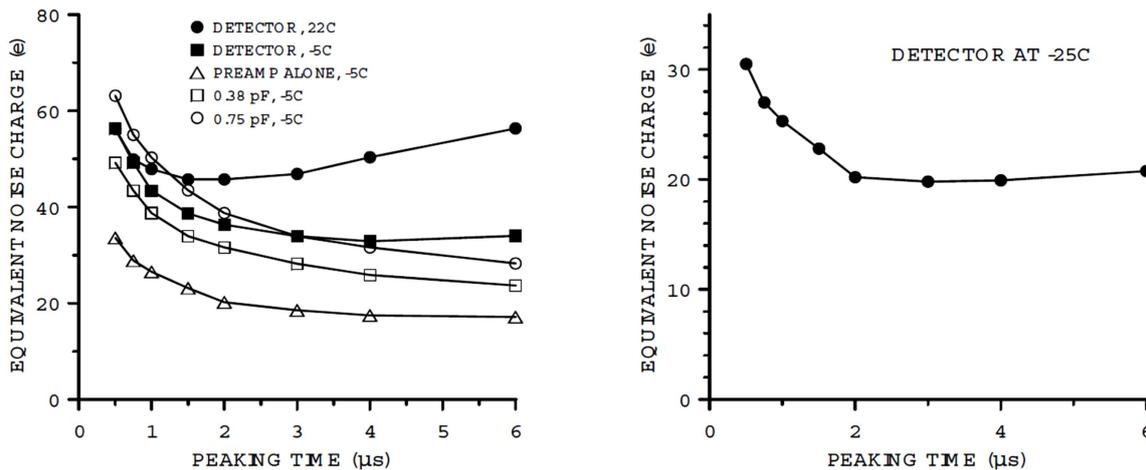


Figure 17. Noise vs peaking time for a high-rate X-ray detector. First prototype (left), and optimized design (right) [5].

Figure 18 shows an X-ray spectrum measured with the system discussed above. The results are comparable with single channel readouts, but with the advantage of achieving high overall data rates through segmentation and parallel processing. This is the key to large-scale detectors at high-luminosity colliders and other applications [5].

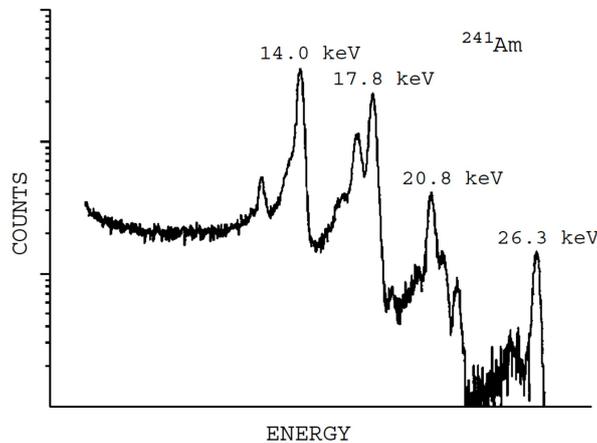


Figure 18. Spectrum measured with the high-rate X-ray detector system [5].

3.2.2 Compton Telescope

There are several techniques to determine the energy and location of Gamma rays. Among them, Compton imaging is one of the most promising; applications range from astrophysics to medical imaging.

Compton telescopes have several advantages. Among them are:

- Possibility to operate at room temperature and achieve a high signal-to-noise ratio by reducing the background to the events that are reconstructed [9].
- Compton telescopes or Compton cameras have a range of several tens of keV to several MeV [10].

As previously stated, both, good energy resolution and good position resolution, are very important to achieve a Compton reconstruction that has high levels of accuracy [10].

Figure 19 shows a basic concept of the Si/CdTe Compton camera. Here, double-sided silicon strip sensors are used as scatterers and CdTe pixel detectors are used as absorbers [10].

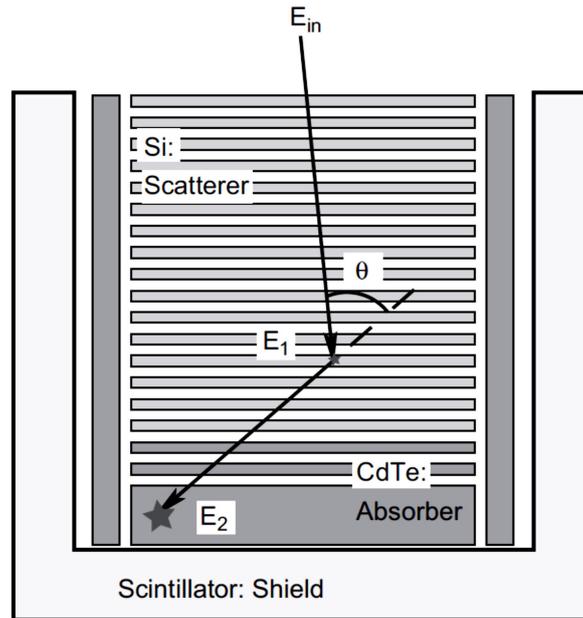


Figure 19. Schematic picture of Si/CdTe semiconductor Compton camera [10].

The Compton camera shown in figure 19 is able to determine the energy of the incident gamma ray. The method used for that is based on the measuring of the Compton scattering point, recoil electron energy, and scattered gamma-ray energy and position relative to the Compton scattering point. The direction of the incident gamma-ray is possible to determine using a cone defined by these measurements [10].

The combination of Silicon and CdTe is suitable for gamma rays ranging from several tens of keV to a few MeV. Because of the small atomic number of silicon, the photo-absorption cross-section is small and it works better than other materials in terms of the 'Doppler broadening' effect. On the other hand, due to the high atomic number of CdTe, it has high photo-absorption efficiency for gamma-rays in this energy region [10].

4 Key Parameters of Strip Sensors

One important parameter to take into account in silicon microstrip detectors is the capacitance. In double-sided AC coupled silicon microstrip detectors, the signal to noise ratio is function of the detector's capacitances. For example, the coupling capacitance has a direct influence on the signal strength, and the interstrip and body capacitances affect the noise level of the signals. Additionally, it is important to note that the resistance of the metal strip can influence the signal strength when using fast shaping [11].

One key parameter that determines the capacitances is the geometry of the strips. Narrow strips minimize the interstrip capacitance. Additionally, lowering of the interstrip capacitance is achievable by p-blocking strips. In AC coupled detectors, wide strips increase the coupling capacitance between the implant and the metal. This at the same time decreases the resistance of the metal strip, which has to be minimized in order to reduce the dispersion of the signal [11].

The precision in the measurement of position depends mainly on the strip spacing and the method of readout. Typical strip pitches range from twenty to few hundred micrometres. At the same time, an important improvement of the measurement precision is gotten with analog readouts if the strip pitch is small enough so that the signal charge (due to diffusion) is collected on more than one strip. In this case, the precise coordinate of the interaction point can be found by the centre of gravity of the signal [4].

As the detectors act as an extended network of resistors and capacitors, they exhibit strong frequency dependence. The implant strip and the metal strip can be represented as a series of finite but small resistors with distributed capacitors to the other electrode, the neighbouring strips and the back plane [11].

A good way to reduce the number of readout channels connected to the readout amplifiers is charge division readouts. The charge collected at the interpolated strips is divided between the two neighbouring readout channels according to the relative position. This can be accomplished by resistive or capacitive division. However, the resistors will contribute to the noise and therefore degrade the position resolution, so the capacitive charge division is preferred (Figure 20). It takes the advantage of the built-in interstrip capacitances that are present automatically due to the geometrical structure of the device. The charge collected at the interpolation strips is divided according to the ratio of the series of interstrip capacitances to the neighbouring readout strips into the two readout channels. The strip-to-ground capacitances are typically an order of magnitude smaller than the interstrip capacitances. These capacitances and the capacitances between non-neighbouring strips distort the linearity of the charge division, extend the signal cluster above two strips, and lead to a position-dependent loss of the collected signal [4].

As seen before, the capacitances play a key role in the performance of strip detectors. The capacitance seen by the amplifier is crucial, and should be small enough in order to obtain small noise, and in the case of charge division, small fraction of charge lost to ground in the capacitive network of readout, floating interpolation strips and backplane. To keep small losses, large interstrip capacitances are desirable; however, this is in contradiction to the requirement of low capacitive load at the amplifier input [4].

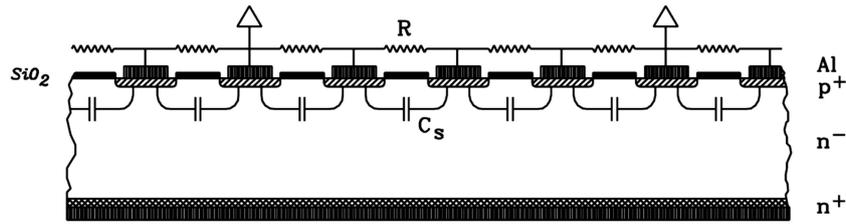


Figure 20. Strip detector with capacitive charge division [4].

Other features to take into account are efficiency and noise signal. These parameters may put limits to capacitive load from the detector to the readout electronics, limiting the length of the detector strip. Additionally, constraints from reliability and stable operation of the detector limit the high electric fields in the detector [4].

One of the most important advantages of the capacitively-coupled readouts is the shielding of the electronics from dark current, which with direct coupling can produce pedestal shifts, reduction of the dynamic range, and may even drive the electronics into saturation [4].

4.1 Coupling Capacitance

An example of the experimental and simulated results for the coupling capacitance of p-side detectors is shown in figure 21 [11].

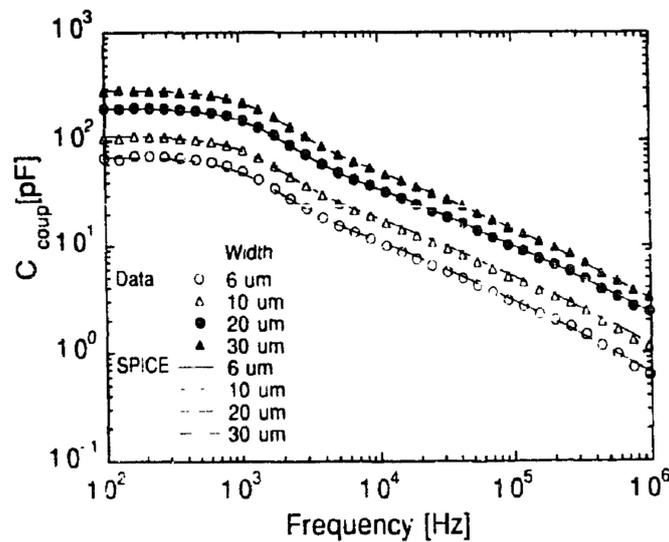


Figure 21. Coupling capacitance for different p-strip widths as a function of frequency (measurements and SPICE simulation) [11].

From figure 21 it is possible to see that the detector capacitances have a strong frequency dependence taking into account that it behaves as a network of resistors and capacitors. Here for frequencies higher than 1 kHz only a small length of the p-implant contributes to the capacitance, thus the observed capacitance is reduced [11].

4.2 Interstrip Capacitance

The interstrip capacitance is the main source of noise in strip detectors. As this is mainly a surface effect, it is necessary to carefully check its behaviour under ionizing radiation. Figure 22 shows an example of the experimental and simulated results of using AC interstrip capacitance between one metal strip and the four closest neighbouring metal strips. The polysilicon resistors acts as a high pass filter, shunting low frequencies to ground [11].

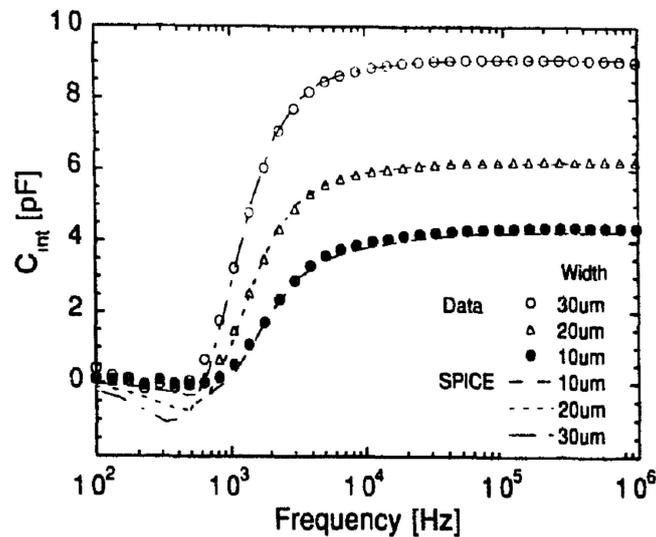


Figure 22. AC interstrip capacitance for different p-strip widths as function of frequency (measurement and SPICE simulation) [11].

4.3 Body Capacitance

The body capacitance of one strip to the backplane is important because its voltage dependence is used to determine the depletion voltage. Figure 23 shows an example of the experimental and simulated results of the body capacitance of a strip detector. It can be seen from the figure that the capacitance is frequency dependent; when the frequency is about 100 kHz, the body capacitance is only 83% of the extracted value [11].

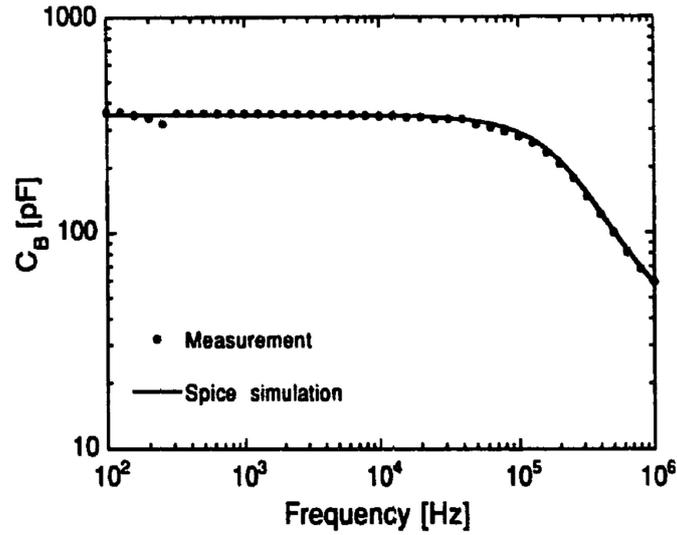


Figure 23. Body capacitance after depletion for a p-type detector as a function of frequency (measurement and SPICE simulation) [11].

4.4 Total Capacitance

Figure 24 shows an example of the experimental and simulated results of the total capacitance for p-side silicon detectors with different strip width but constant strip pitch of 50 μ m, as function of the ratio strip width over pitch w/p . As mentioned earlier, a reduced strip width lowers the total capacitance [11].

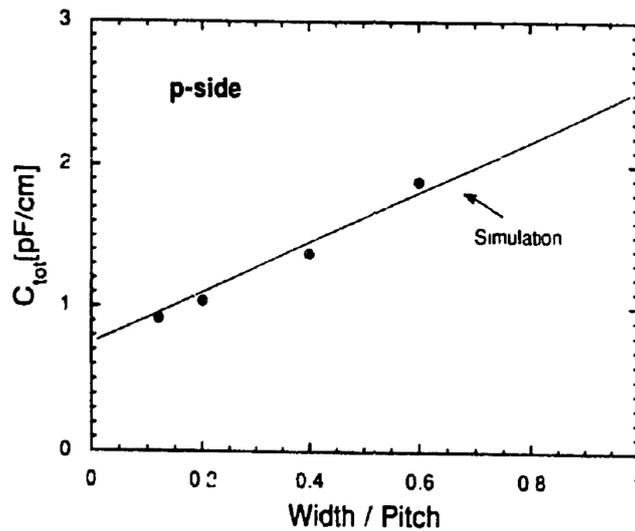


Figure 24. Total capacitance for a 50 μ m pitch p-side detector as a function of the ratio width over pitch w/p [11].

The total strip capacitance has a key role because it contributes to the noise of the front-end amplifier. The total strip capacitance generates noise like a discrete capacitor. The metal strip of each channel has finite resistance (e.g. $30\Omega/\text{cm}$ for $10\mu\text{m}$ width) and does not contribute to the noise of the fast amplifier [11].

The design of strip detectors is a challenge for the manufacturers. To optimize the geometry, the width of the implant and the metal has to be decreased to minimize parasitic capacitances, but at the same time increased to maximize the coupling capacitance and minimize the resistance. Additionally, the oxide layer thickness has to be decreased to maximize the coupling capacitance, but increased to maximize the breakdown voltage [11].

4.5 Interstrip Resistance

The interstrip resistance is one of the most important parameters that characterize the quality of microstrip detectors. Basically, the interstrip resistance along with the interstrip capacitance determine the number of strips involved in the charge distribution when ionizing radiation interacts with the detector [12].

Additionally, the interstrip resistance at the ohmic contact shows the quality of the p^+ stop structure. On the other hand, the interstrip resistance value let us determine important parameters as depletion voltage, n^+ strip separation voltage, as well as detection of technological defects during the fabrication of the strips [12].

Finally, variation in the value of the interstrip resistance show us the effects of different factors, as the ionizing radiation, defect content in silicon, etc. [12].

5 Charge Sensitive Amplification

Figure 25 shows a detector connected to an amplifier with very high input resistance.

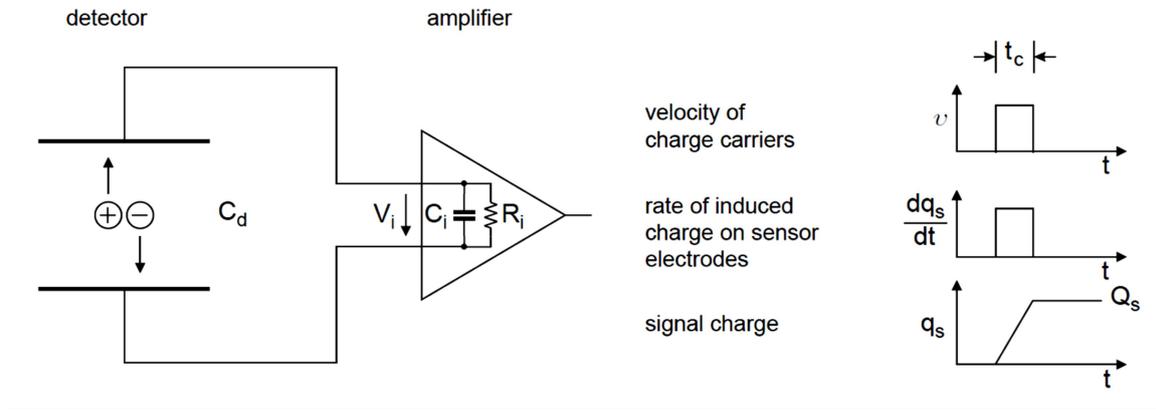


Figure 25. Charge collection and signal integration in an ionisation chamber [8].

The sensor electrodes form a capacitor C_d . C_i represents the dynamic input capacitance. When mobile charge carriers move towards the electrodes, they change the induced charge on the sensor electrodes. Supposing that the amplifier has a small input resistance, the time constant $\tau = R_i(C_d + C_i)$ that discharges the sensor is small too, and the amplifier will sense the signal current. On the other hand, if the input time constant is large compared to the duration of the current pulse, the current pulse will be integrated on the capacitance, and then the resulting voltage at the amplifier input is [8]:

$$V_i = \frac{q_s}{C_d + C_i} \quad (1)$$

It is important to mention that the magnitude of the signal is dependent on the sensor capacitance, as seen on equation 1. In that case, in a system containing a sensor varying its capacitance, varying strip lengths or a partially depleted sensor where the capacitance vary with the applied bias voltage, it is necessary to deal with additional calibrations. However, if it is used a charge sensitive preamplifier, it would overcome this problem providing an output signal amplitude independent of the input capacitance [8].

Figure 26 shows a circuit configuration of a charge sensitive preamplifier.

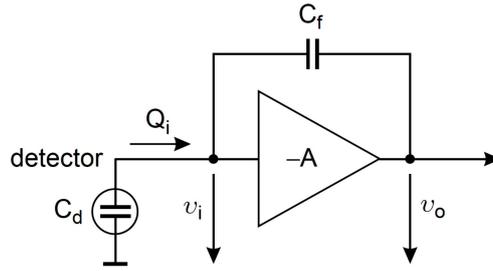


Figure 26. Principle of a charge-sensitive amplifier [8].

The sensor capacitance is discharged by the resistive input impedance of the feedback amplifier with the time constant [8]:

$$\tau_i = R_i C_d = \frac{1}{\omega_0 C_f} \cdot C_d \quad (2)$$

From equation 2 it can be seen that the rising time of the charge sensitive amplifier increases with the sensor capacitance. The amplifier response can be slower than the duration of the current pulse from the sensor, due to the charge initially stored on the detector capacitance, but the amplifier must be faster than the peaking time of the subsequent pulse shaper. The feedback capacitance must be much smaller than the sensor capacitance. For example, for a capacitance $C_f = C_d/100$, the gain bandwidth product must be $100/\tau_i$, which means that for a rise time constant of 10 ns the gain bandwidth product must be $\omega = 10^{10} \text{ s}^{-1} = 1.6 \text{ GHz}$ [8].

Another important parameter in position sensitive detectors is the input impedance. Typical input impedance of charge sensitive amplifiers in strip detectors systems is of order $\text{K}\Omega$. Fast amplifiers designed to optimise power dissipation have input impedances in the range of 100 to 500Ω [8].

Figure 27 shows a silicon strip sensor and its readout as a bank of amplifiers. C_b represents the capacitance of each strip to the backplane and C_{ss} represents the fringing capacitance to the neighbouring strips. If the amplifier has infinite input impedance, the charge induced on one strip will be capacitively-coupled to the neighbours and the signal will be distributed over many strips, according to C_{ss}/C_b . On the other hand, if the input impedance of the amplifier is low compared to the interstrip impedance, almost all the charge will flow into the amplifier of one channel, and the neighbour channels will show only a small signal [8].

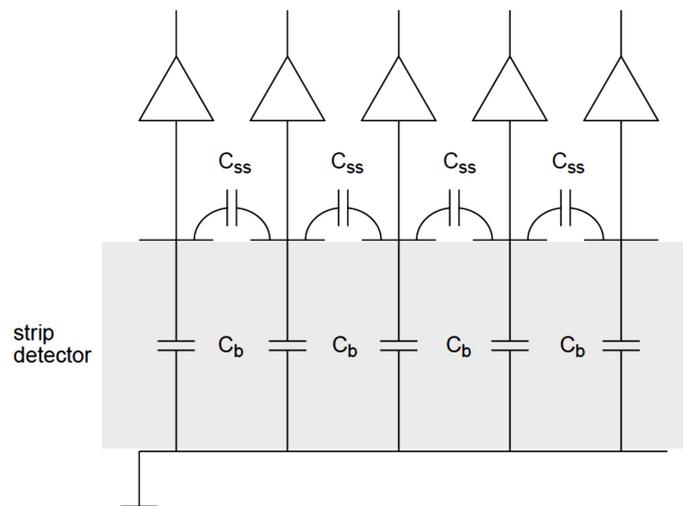


Figure 27. To preserve the position resolution of strip detectors the readout amplifiers must have a low input impedance to prevent spreading of signal charge to the neighbouring electrodes [8].

As mentioned earlier, the signal to noise ratio for a given signal charge is inversely proportional to the total input capacitance. At the same time, this dependence is a general feature that is independent of the amplifier type [8].

6 Noise Analysis of Sensor and Front-End Amplifier

Figure 28 (left) shows a model of the detector's front end electronics used to determine how the pulse shaper affects the signal to noise ratio. Here, the capacitance C_d represents the detector side, as this is a relevant model to represent many radiation sensors. The bias voltage is applied to the sensor through the resistor R_b . The bypass capacitor C_b shunts any external interference coming through the bias supply line to ground. This capacitor behaves as a low impedance for high frequency signals, so for the sensor signals the other side of the bias resistor is connected to ground. At the same time, the coupling capacitor C_c or 'blocking capacitor' blocks dc voltage, in this case the bias voltage, from the amplifier input.

The series resistor R_s represents all the resistances present in the connection from the sensor to the amplifier input, including the resistance of the sensor electrodes, the resistance of the wire-bonds and PCB traces, any input resistance used to protect the amplifier against large voltage transients, and parasitic resistances in the input transistor [8].

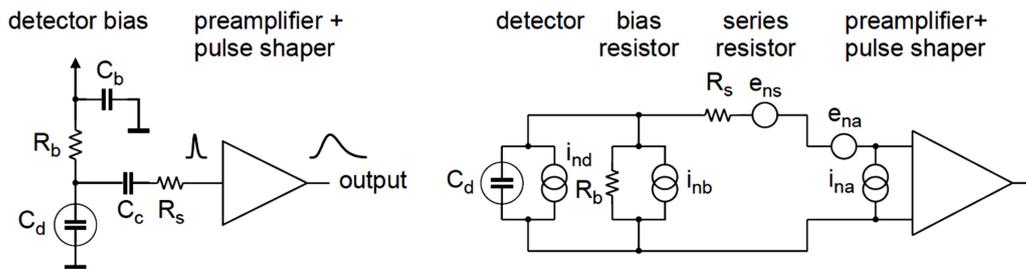


Figure 28. A detector front-end circuit and its equivalent circuit for noise calculations [8].

It is important to clarify the real role and constraints of the bias resistance. It is often thought that the signal current generated in the sensor, due to its interaction with ionizing radiation, flows through R_b and then, the resulting voltage drop is measured. If the time constant $R_b C_d$ is small compared to the peaking time of the shaper τ_p , the sensor is discharged through R_b and much of the signal is lost. To solve this situation it is necessary to ensure that $R_b C_d \gg \tau_p$, or $R_b \gg \tau_p / C_d$. The bias resistor must be large enough to block the flow of the signal charge, and to have the entire signal available for the amplifier [8].

Figure 28 (right) also shows the equivalent circuit for the noise analysis, including both, current and voltage noise sources. The shot noise i_{nd} produced by the sensor leakage current is represented by a current noise generator in parallel with the sensor capacitance. The resistors can be modelled either as voltage or as a current generator. It is common to use noise current sources to represent resistors shunting the input, and noise voltage sources to represent resistors in series with the input [8].

Shaping time is an important parameter for every readout system based on semiconductor detectors; that includes clearly the strip detectors. In that context, it is a must to understand its effect over the signal to noise ratio.

Figure 29 shows how the shaping time affects the equivalent noise charge ENC. Here it can be seen that at short shaping times the voltage noise dominates in the signals, whereas at long shaping times the current noise dominates. At the same time, it is possible to see that the minimum noise is obtained where the current and the voltage contributions are equal. At this point the minimum noise is flattened by the presence of the $1/f$ noise [8].

Finally, the figure 29 shows that an increase in the detector capacitance generates an increase of the voltage noise contribution, shifting the minimum noise point to longer shaping times and increasing in the minimum noise value [8].

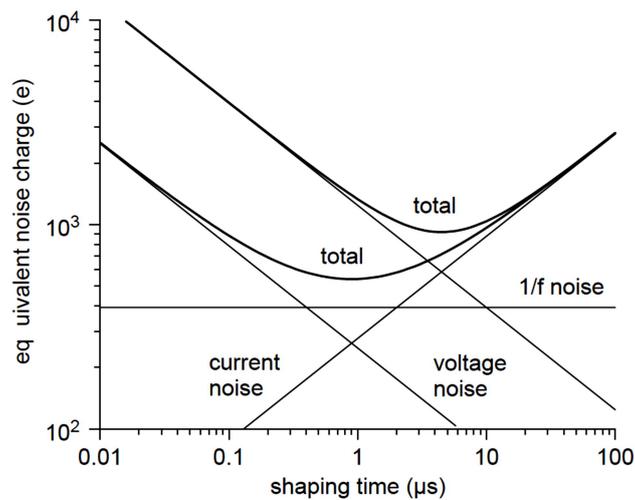


Figure 29. Equivalent noise charge versus shaping time. [8].

7 Overview of the Readout System

7.1 Strip Sensor (SINTEF)

The sensor chosen for this thesis is a custom made strip sensor from the Norwegian company SINTEF, produced in framework of the project AEGIS [13]. Figure 30 shows the layout of the sensor, whilst figure 31 shows a zoomed in image of its bottom left corner.

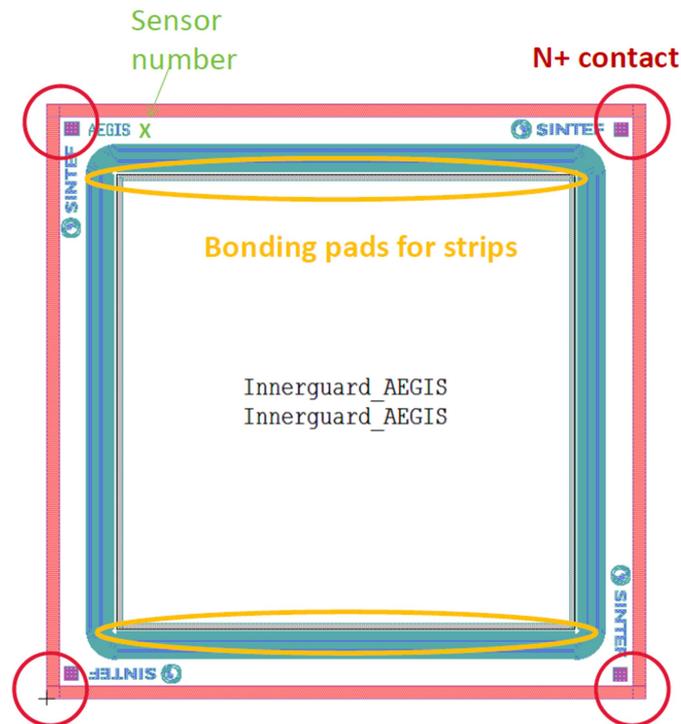


Figure 30. Strip sensor layout from SINTEF [14].

The sensor contains 128 strips with a pitch of $80\ \mu\text{m}$. It was fabricated in a $300\ \mu\text{m}$ thick Silicon wafer but its active area was reduced to $200\ \mu\text{m}$ to provide the possibility to fill the etched area with any kind of convertor for the detection of non-charged particles. The bonding pad openings of the detector are $100 \times 50\ \mu\text{m}^2$ and it contains frontal side contacts for the bias voltage [14].

Despite the size of the detector is just $14 \times 14\ \text{mm}^2$ and its active area is only $10 \times 10\ \text{mm}^2$ [14], it fulfils the basic needs of the thesis and its output parameters are within the range of input requirements of the front-end electronics.

The advantage of having a small strip detector for the debugging and testing of the system is that the risk of damage due to crashing of the wire-bonds is smaller, and at the same time, the manipulation is easier due to a smaller PCB. However, it is important to highlight that the core of the hardware and firmware designed to drive this small strip sensor can be used for

driving bigger strip sensors, so that minor changes are needed when dealing with different applications.

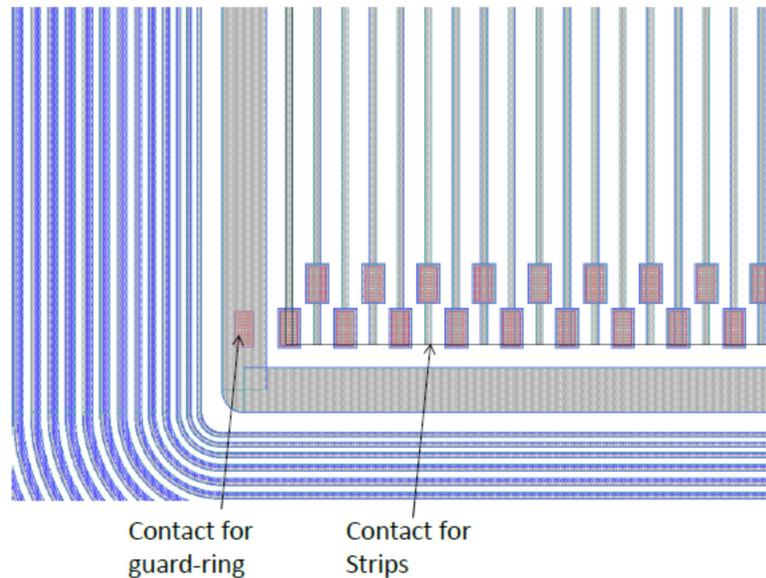


Figure 31. Bottom left detail of the strip sensor from SINTEF [14].

7.2 Front-End Electronics - ASIC (BNL)

As it was mentioned in the previous sections, front-end electronics has a key role in any detector system. Since this electronic part is directly in contact with the sensor's channels, it must be carefully designed to avoid degrading the sensor's analog signals and hence, deteriorating substantially the energy resolution. In systems composed of tens, hundreds or even thousands of channels the fabrication of front-end electronics using discrete components cannot be considered as realistic. A better solution is to contain these sensitive electronics into a single chip that can deliver already processed data through standard digital signals and/or amplified analog signals.

The ASICs or Application-Specific Integrated Circuits contain all the necessary electronics to interact directly with the sensor causing minimum interference to it. They have the advantage of containing tens or hundreds of readout channels confined in a small area of semiconductor material (few millimetres) thanks to the high technology of microelectronics available nowadays.

Even though the ASICs are by nature designed and optimized for a particular application and sensor [15], it is possible to avoid the very high cost of a custom design by taking advantage of already fabricated ASICs which were intended for similar purposes. This is the case of the ASICs used in this thesis; they were previously designed by the Instrumentation Division Group of the Brookhaven National Laboratory (BNL) in New York, USA.

The ASICs, documentation and support were provided as part of a scientific collaboration. Figure 32 shows a picture of the ASIC.

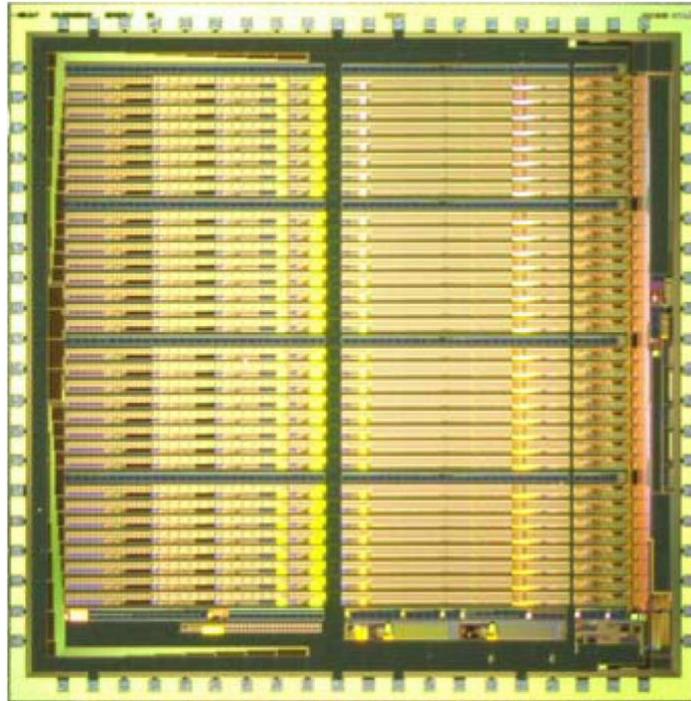


Figure 32. 5x5 mm bare readout ASIC from BNL [9].

Each ASIC contains 32 front-end channels. Each channel contains a low noise charge preamplifier with fully compensated continuous reset, 5th order shaping amplifier with complex conjugate poles, a peak amplitude detector with analog memory, a band-gap referenced baseline stabilizer, a single threshold discriminator, and a calibration capacitor [16], as shown in figure 33.

Common to all channels, the ASIC contains two 10-bit DACs; one to coarsely control the threshold level and the other to control the amplitude of the test pulse applied to each channel through the test capacitors. Additionally, it contains the necessary circuitry to interface the ASIC with the external driving electronics [16].

Each channel has a 4-bit DAC for fine equalization. Channel gain can be selected as: 14.25, 28.5, or 57 mV/fC, covering an energy range up to 3.2 MeV. The shaping time can be set to 4 different values: 500 ns, 1 μ s, 2 μ s, 4 μ s. Additionally, the polarity to which the channels are sensitive to can be chosen (positive or negative) [16].

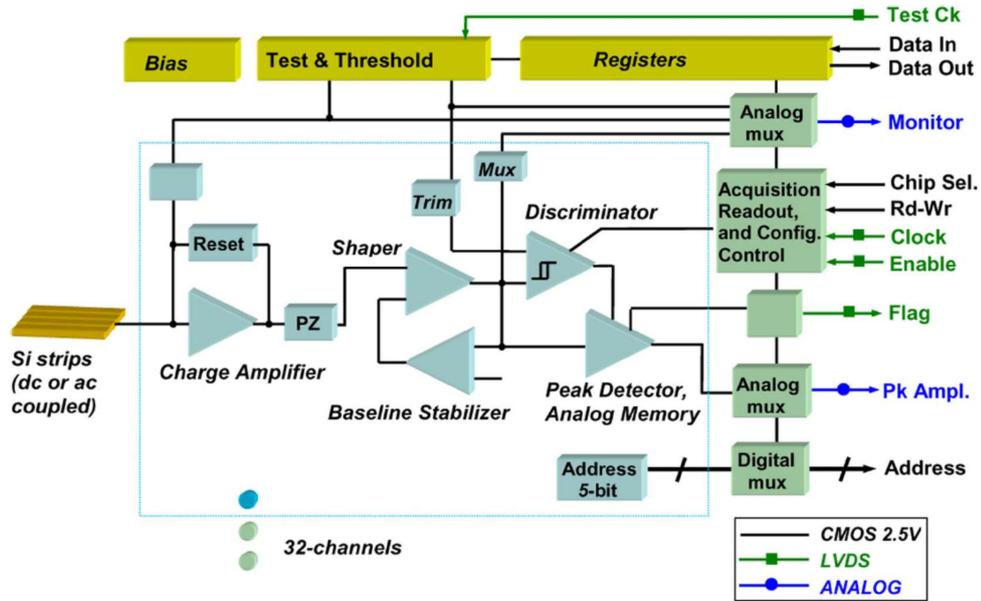


Figure 33. Architecture of the 32-channel ASIC from BNL [9].

The ASIC operates in three different modes: Writein, Acquisition and Readout.

The Writein is the mode in which the ASIC is configured by writing its configuration register. This register is 234-bit long and its access is serial through a 234-bit fast shift register (FSR) [16]. Figure 34 shows the timing diagram of the Writein mode.

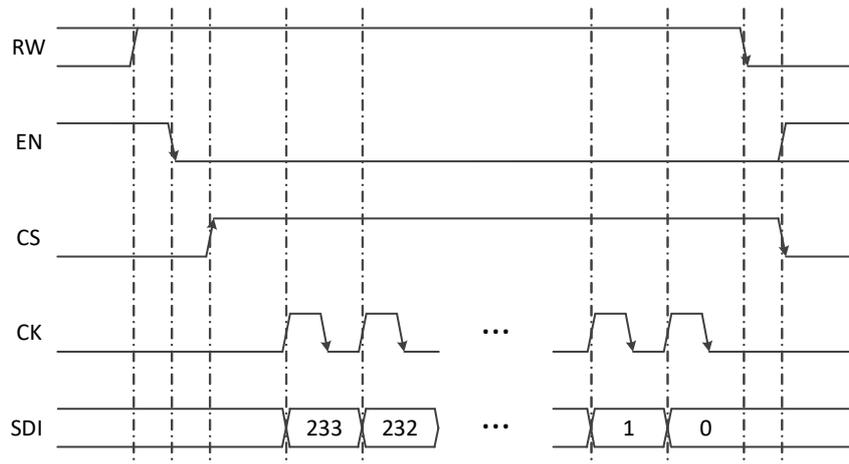


Figure 34. Timing diagram of the Writein mode.

The acquisition is the mode used to make the ASIC’s channels sensitive to charges delivered by the sensor. The signal generated in each channel by the electronics due to the charge, must be higher than the threshold in order to be taken into account by the peak detector. On the

contrary, the event is simply discarded. The valid events are saved in an analog memory [16]. Figure 35 shows the timing diagram of the Acquisition mode.

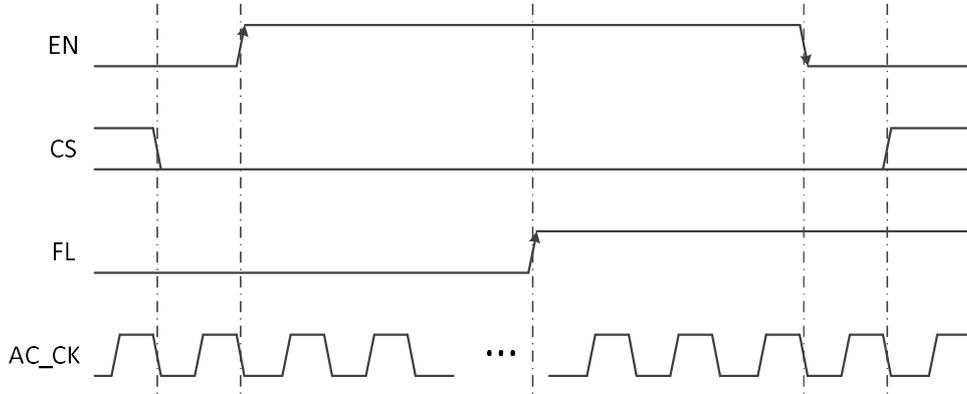


Figure 35. Timing diagram of the Acquisition mode.

Finally, the Readout mode is used to read the information about valid events saved in the ASIC. That information consists of the analog amplitude of the event in a channel and its correspondent digital address. The reading process is made in sparsified mode, which means channel by channel [16]. Figure 36 shows the timing diagram of the Readout mode.

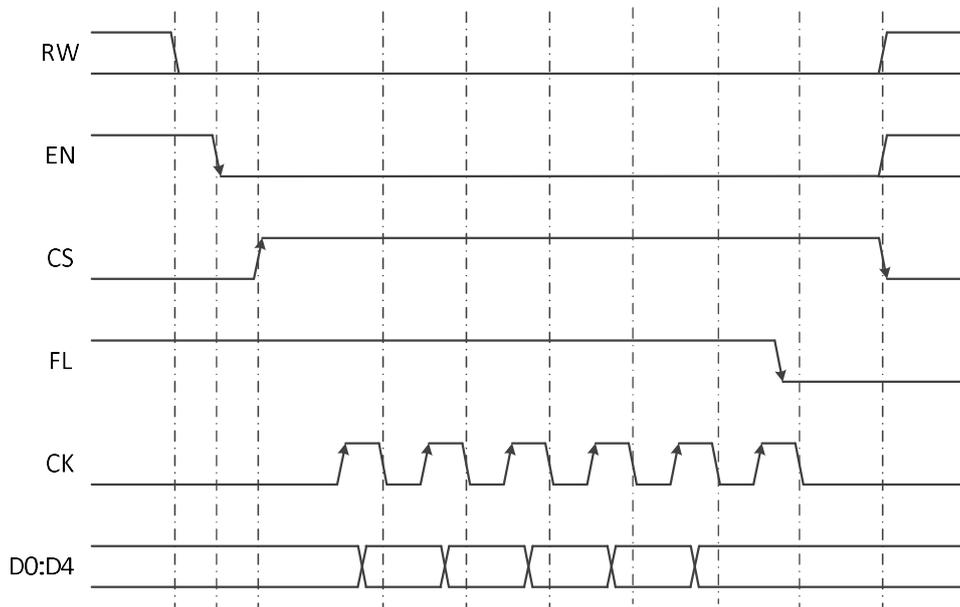


Figure 36. Timing diagram of the Readout mode.

7.2.1 Global Threshold DAC

The global threshold is designed to help readout electronics to work out of the noise range, but at the same time it can be used to remove events produced by particles which are not of interest during a measurement. The threshold value, which is an analog global value for all the channels of a particular ASIC, is produced internally by means of a Digital to Analog converter DAC [16]. Figure 37 shows a simplified sketch of the global threshold.

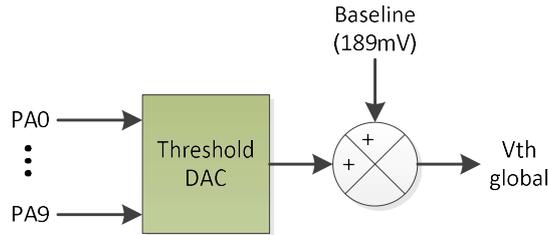


Figure 37. Simplified diagram of the global threshold circuit.

Aforementioned, the ASIC's global threshold is controlled by a 10-bit DAC. The DAC has its own baseline (different than channel's baseline), approximately equal to 189mV, to which values set in the DAC are summed up. Consequently the minimum value set in the DAC (0:0) corresponds to the baseline. The threshold DAC step is about 1.95mV, giving the possibility of setting the global threshold value up to approximately 2.19V (including the baseline) [16]. A simple equation to calculate the global threshold value is shown below:

$$Vth_{global} = BL_{thD} + N_{thDAC} * DAC_{thste} \quad (3)$$

where BL_{thDAC} is the baseline of the threshold DAC, N_{thDAC} is the digital value set in the DAC, and DAC_{thstep} is the DAC step value.

7.2.2 TRIM DAC

Even though there is a global threshold value, the actual threshold level for each channel is slightly different due to fabrication and technological reasons. In that case, in order to set the sensitivity of every channel to approximately the same level, it is necessary to equalize the threshold value of each channel. This is done with the help of a 4-bit trimming DAC available in each channel. The trim DACs have a step value of 3.5mV, giving a maximum correction value of 52.5mV [16]. The trim DAC value of a particular channel can be calculated using the equation below:

$$Vtrim_{chDAC} = (15 - N_{ch_{trimDAC}}) * DAC_{trimstep} \quad (4)$$

where $N_{chtrimDAC}$ is the digital value set for a particular channel's DAC, and $DAC_{trimstep}$ is the trimming DAC step value.

As it is seen in equation 4, the trim DAC logic of every channel works inversely to the global threshold DAC, having its maximum value at 0:0, and its minimum value at 1:1.

Using equations 3 and 4, the actual threshold of any channel can be express as:

$$V_{th_{ch}} = V_{th_{global}} - V_{trim_{chDAC}} = BL_{thDAC} + N_{thDAC} * DAC_{ths} - (15 - N_{ch_{trimDAC}}) * DAC_{trimstep} \quad (5)$$

Additionally, equation 5 shows that the values set in the trim DACs are always subtracted from the global threshold value.

The sensitivity of a channel can be defined as the minimum detectable energy set by the channel's actual threshold level respect to its baseline. In that sense, and according to equation 5, the trim DACs help to equalize the system's channels to have sensitivity equal or similar to the most sensitive channel (reference channel).

In order to have a clear idea about the meaning of equation 5, Figure 38 shows a simplified diagram of the threshold circuit used in every channel.

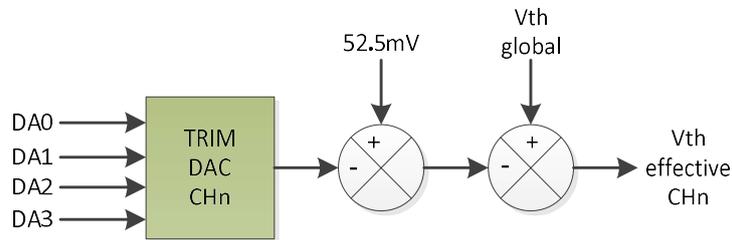


Figure 38. Simplified diagram of channel's threshold circuit (effective threshold).

The trimming DAC cannot be considered as a fine tuning for a channel's threshold since it has a bigger step compared to the global threshold DAC's, however, they do help to make the system more uniform in terms of sensitivity.

7.2.3 Energy Ranges

Three different energy ranges are available in the ASIC. Each range is chosen by the selection of its corresponding gain value: 14.25mV/fC provides an energy range up to 3.2MeV, 28.5mV/fC up to 1.57MeV, while for 57 mV/fC the maximum energy value is about 788 keV, theoretically [9].

Eventhough the maximum energy range of the ASIC can be used always, it is recommended to choose the range according the energy of the particles of interest; this is because it will provide a more precise result and hence a better energy resolution. For example, if low energy is to be measured (below 788 keV) it is recommended to use 57mV/fC; the reason is that the maximum output signal from the ASIC (2V) will be divided by a smaller energy range, giving more precise values. On the other hand, if heavy particles are wanted (higher than 1.57MeV), it is necessary to use the lower gain, otherwise, the energy of the particles will saturate the ASIC's channels. For measuring particles with energies in the range 788 keV to 1.57MeV, the middle range is recommended.

Additionally, four different shaping times can be selected according to the activity of the radioactive source. Longer shaping time can reduce the noise of the measurement when there is not parallel noise contribution to the ASIC's channels [17]. On the other hand, a short shaping time can reduce considerably the measurement time. This is very important because photons are typically used for calibration and since the efficiency of silicon detecting photons is very low, long measurement times are needed in order to have enough statistics; choosing the shortest shaping time saves hours of measurement time, and even more important, reduces the human exposure to radiation.

Having several energy ranges is an advantage in terms of resolution, however, it makes the full calibration of the device very time consuming: every combination of gain-shaping time must be individually baseline-scanned, equalized and calibrated; in other words all the three analyses must be performed for 12 different possibilities (3 gains + 4 shaping times). In the present work, the baseline scan and equalization was performed for all 12 scenarios, but since it is not easy to find calibration sources providing well defined energy peaks in all the ranges, the calibration was only performed for the 2 more useful combinations for this thesis: Gain=14.25 mV/fC - Shaping time=0.5 μ s, and Gain=57 mV/fC - Shaping time=0.5 μ s. These two ranges permit to measure any energy up to 3.2MeV, but with more resolution for energies up to 788 keV, respectively.

7.2.4 Analog Output Signals

The ASIC provides two analog output signals: Peak Detector output (PD) and Analog Monitor Output (OA). The first one contains information about the energy deposited at a given channel and the second one contains information about internal features of the readout channel. The OA signal is basically used to characterize and monitor any channel of the ASIC. Consequently, both analog signals are equally important [16].

In order to better understand the meaning of the PD output values, figure 39 shows an example of the process. It can be seen from the figure that the output signal coming from the internal analog memory, and shown at the PD pin during the readout phase, includes the baseline voltage of the corresponding channel (ideally the same value for all the channels). During the data analysis, the baseline of every read value must be subtracted to obtain the real energy-voltage equivalent value.

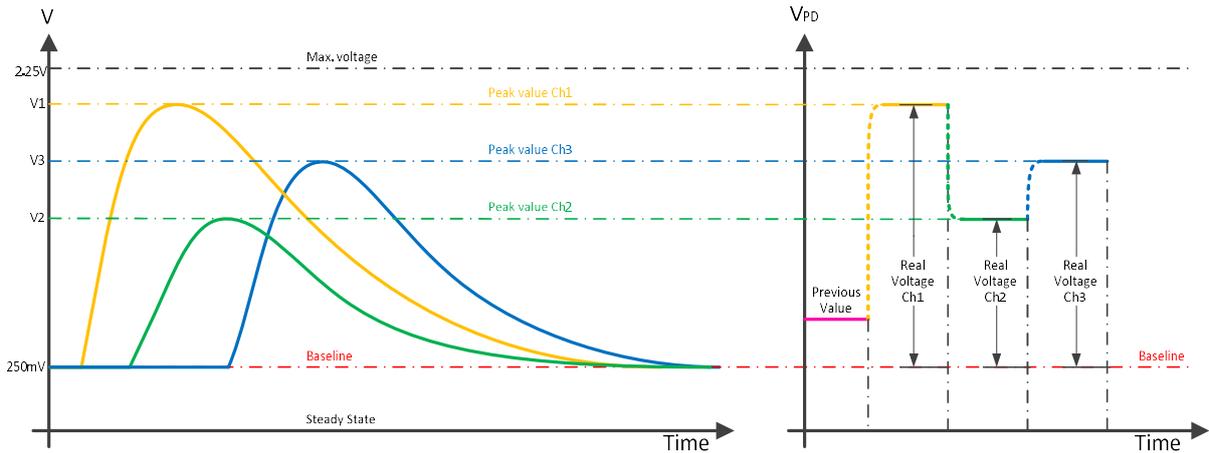


Figure 39. PD signal generation for three channels; Signals at peak detection circuits (left) and PD signal during readout phase (right).

Regarding the OA pin, several internal analog signals can be chosen and displayed at this output. Figure 40 shows a schematic of how the OA pin works.

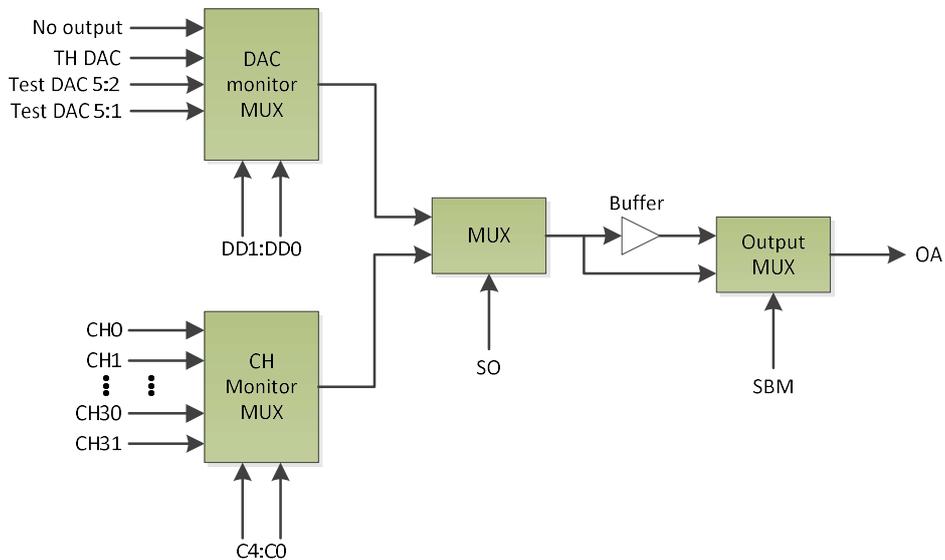


Figure 40. Signal selection circuit of OA pin.

As seen in figure 40, there are several control signals that help choosing the wanted analog signal to be displayed at the OA pin. The first control signal is SO. This control can choose between showing DACs or Channels output. When choosing DACs, one can monitor either the threshold DAC value or the test pulse DAC. When choosing the option Channels, the output of the selected channel’s shaper is displayed. This is a very important feature not only

because one can verify the shaping time and amplitude of the output signal, but because it offers the possibility to measure the channel's baseline value [16]. When measuring the baseline it is imperative to do it in a place free of ionizing radiation and light, avoiding as much as possible interactions with the sensor that disturb the preamplifier's output signal and hence the correct sampling of the baseline.

As it is typical, every channel of one ASIC has a slightly different performance and special procedures must be taken in order to correctly characterise the device. Those procedures will be described in further sections.

One more important point regarding the analog output signals is the settling time. Ideally, when accessing the analog memory one would expect the analog values to be almost immediately available at the PD pin after a clock edge, however in reality, since the analog values are read in sparsified mode and due to the effect of internal capacitances, the analog value at the output of the analog memory changes in time from a previously read or sometimes unknown value until reaching the newly read value; this means that the worst-case scenario is when the output signal goes for a full excursion of the range, as shown in figure 41.

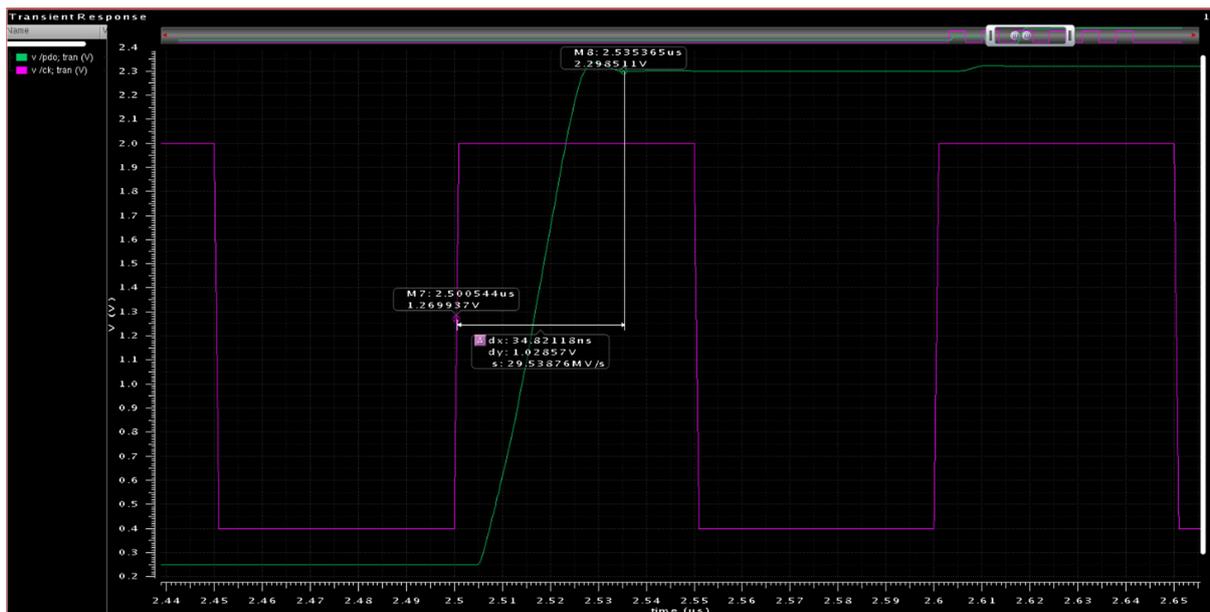


Figure 41. Simulation of the maximum PD transition for a capacitance of 30pF. Pd signal (green), readout clock (purple). Provided by Wenbin Hou – Brookhaven National Laboratory BNL.

As can be seen in figure 41, the maximum settling time of the signal at PD pin is about 35ns. This is an important parameter because it limits the readout speed of the system. Additionally, the delay added by the signal conditioning circuit must be taken into account as well. This will be discussed in more detail in section 10.

Another important point regarding the sensitive analog signals is the impedance that they must drive. Even though there is the possibility to activate an analog output buffer for each

analog signal, the load connected to those pins must be limited to a minimum impedance value; otherwise the output signal will be affected and will show an apparent value which is lower than the real one. Figure 42 shows the effect of different loads connected to PD pin. According to the simulation, a load higher than $4\text{K}\Omega$ provides an error less than 1% in the amplitude of the analog signal.

The load of the PD pin is in fact the signal conditioning circuit. The input impedance of the signal conditioning circuit is $5.4\text{K}\Omega$, ensuring a low amplitude error. On the other hand, a much higher input impedance value would deteriorate substantially the performance of the fast OpAmps in the first stage of the signal conditioning circuit.

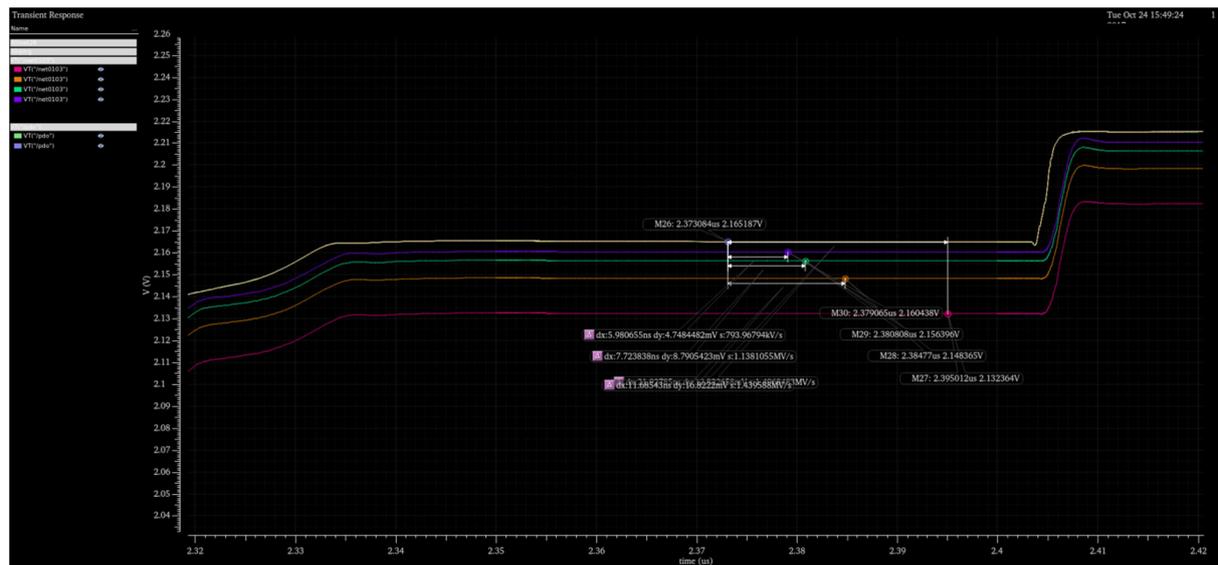


Figure 42. Simulation of attenuation of the PD signal for different loads. Ideal (white), $2\text{ k}\Omega$ (magenta), $4\text{ k}\Omega$ (orange), $8\text{ k}\Omega$ (green), $16\text{ k}\Omega$ (purple). Provided by Wenbin Hou – BNL.

7.2.5 Signal Conditioning Circuit

The main components of the signal conditioning circuit are the active voltage shifter with unitary gain which adjusts the analog signals to cover most of the ADC range and provides adequate impedance loading to the ASIC's analog pins, the unitary gain single to differential amplifier which offers better noise immunity, and the 14-bit fast ADC.

Figure 43 shows a basic sketch of the signal conditioning circuit's structure.

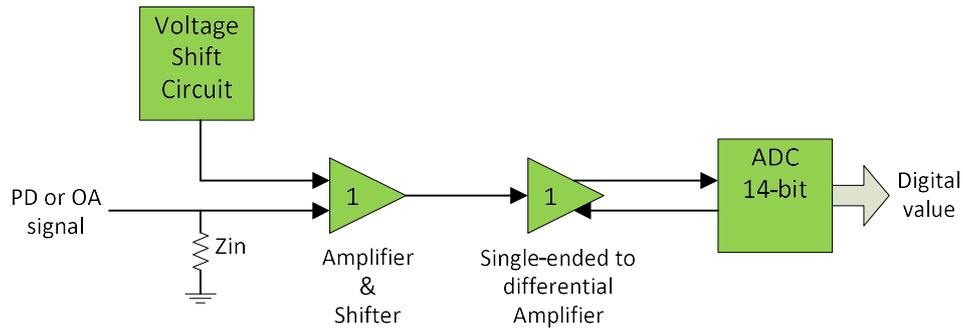


Figure 43. Signal conditioning circuit sketch.

The PD pin of the ASIC has a maximum output voltage equal to 2.25V. Theoretically, the first 250mV of the signal represents the channel's baseline and from 0.25V up to 2.25V corresponds to the voltage range (2V max.) in which the measured energy-voltage equivalent value can be displayed [16], as shown in figure 44.

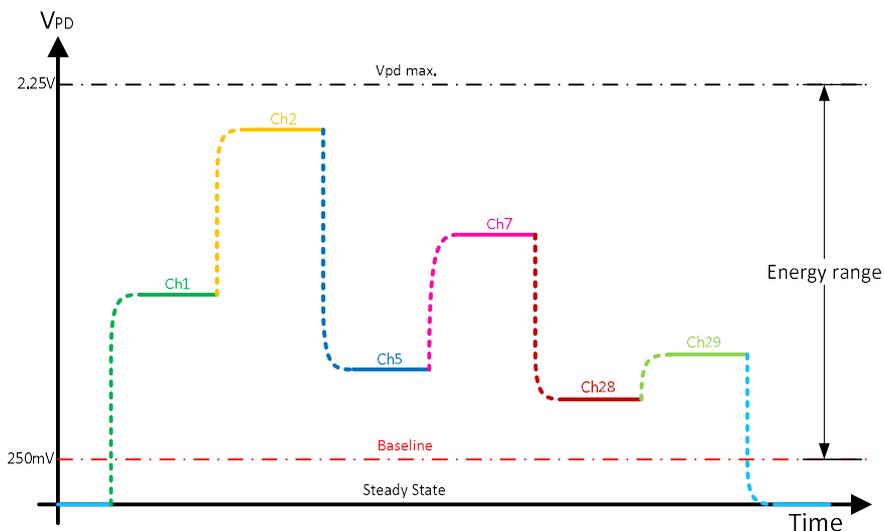


Figure 44. PD signal energy range for 6 channels containing information (before signal conditioning circuit).

Every value contained in the ASIC's analog memory must undergo an external analog to digital conversion in order to safely send it to the PC for post-processing. As it is not likely to have a commercial ADC using a similar input voltage range, it was necessary to include a signal conditioning circuit in the design. Since the signal conditioning circuit manages the most important and sensitive signals of the system, it was used a differential ADC, which means that the analog signal must be converted from single-ended to differential. Differential signals are more robust against external electromagnetic interference which is an important advantage for the system. Common ranges in differential ADCs are either $\pm 0.5V$ or $\pm 1V$. In

this case, the $\pm 1V$ range matches the real voltage range produced by the interaction of a particle without counting the baseline value.

Even though no amplification of the analog signal is needed, a shift of the ASICs' analog signals is necessary just before the analog to digital conversion. This is done in order to use as much as possible the full range of the ADC. Figure 45 shows how the output analog signals shown in figure 44 are re-arranged by the signal conditioning circuit.

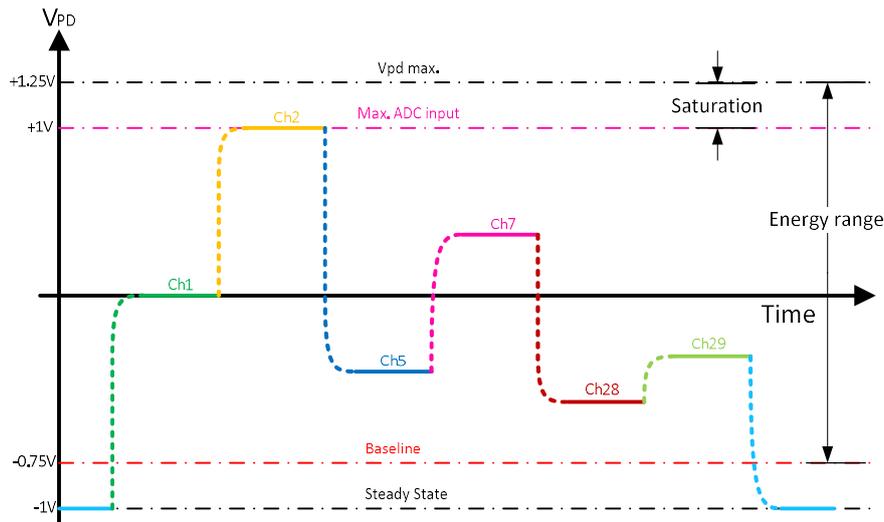


Figure 45. PD signal after signal conditioning circuit.

According to figure 45, the zero output level will be shifted to about $-1V$ and the maximum PD voltage will be about $+1.25V$. Since the maximum positive ADC's input value is $+1V$, signals with amplitude between $+1V$ and $+1.25V$ saturate the ADC. In the case that the particles of interest generate signals in the saturation part of the range, a higher energy range must be selected by changing the amplification factor of the ASIC.

There are important factors that can influence the desired performance of the signal conditioning circuit and hence the resolution of the system. Usually, a good selection of the OpAmps minimizes most of the problems, however due to the nature of the ASIC's analog signal which is based on a series of constant voltage levels, some characteristics become important; examples are: tolerance of discrete passive components, offset added by active components, OpAmps' SNR, etc. Specifically speaking about the offset produced by the OpAmps and tolerance of passive components, the ADC input will be provided with analog values apparently either higher or smaller than the real ones. Fortunately, the ASIC counteracts these effects by providing energy-voltage equivalent values which are referenced to the channel's baseline. This is very important because previously knowing the baseline value of each channel, the apparent offset is eliminated.

Additional issues affecting the signal conditioning circuit, like different gain values due to the tolerance of the discrete components or no linearity of the amplification chain, are counteracted by the calibration of the channels.

7.2.6 Digital Output Signals

Information recorded in the ASIC about the energy of the events is given by the PD analog signal, however this is not the only important information; it is necessary to know the position of the channels that those energies belong to. That information is provided by the digital address signals. During the readout phase, each analog value is delivered with its corresponding channel's digital address [16].

Even though analog and digital signals are output by the same clock edge, their delays are different. The analog signal by nature takes much more time to settle, while the digital signal is available within few nanoseconds. In the case of the digital output, the delay is small enough to make possible reading of addresses at maximum speed (50MHz), but in the case of the analog signal this is not possible. As a consequence, the speed of the readout process is limited greatly by the analog settling time. In any case, the digital signal delay is a parameter that must be taken into account in the timing constraints in the firmware design. Figure 46 shows the time delay for one bit of the address register.



Figure 46. Delay of the address bit D0 for a capacitive load of 20pF and for a clock frequency of 10 MHz.
Provided by Wenbin Hou – BNL.

In the simulation shown in figure 46 it is visible a common situation in MOS-based circuits: the delay of rising and falling edge is different; This is due to different RC constants associated to the MOS switches involved in each transition; then the value taken in the firmware design was the higher one, which is not more than about half clock cycle.

Another no less important digital output signal to consider is the events' flag FL. This signal informs about the occurrence of at least one valid event counting all the channels of the ASIC. This is basically an ORed signal of all the channels' flags [16]. Eventhough this is a digital signal, its delay is much higher than the one of the digital address because it depends directly on the shaping time of the analog signals plus the delay of the peak detectors and other internal logic circuits. Figure 47 shows a simulation of this signal.

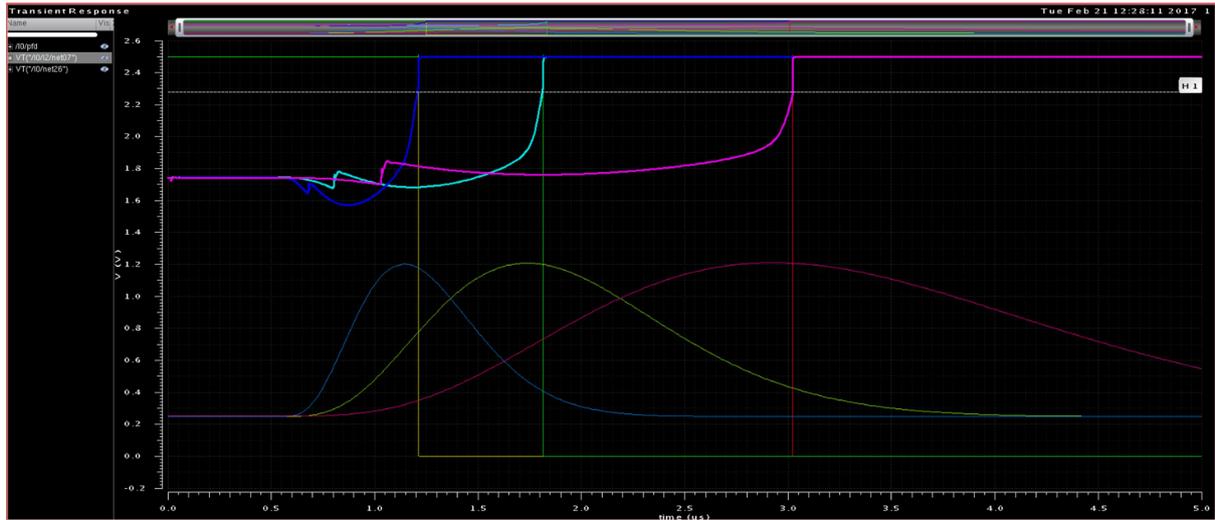


Figure 47. Three peaking times: 500ns, 1us, 2us (down) and their respective flag delay (up). Provided by Wenbin Hou – BNL.

During the acquisition phase, if any valid event was recorded, the flag is automatically asserted. Then, during the readout phase the flag lowers when all the recorded events were readout [16]. The delay of this signal is very important because, as in the case of the analog signal's delay, it limits the maximum readout speed. If not given enough time to the flag to change, the last event could be mistakenly readout twice.

From figure 47 it is visible that the delay of the flag is shaping time-dependent; the longer the shaping time, the longer the delay is. Here we can see that the delays range from about 50 ns (shaping time=500 ns) to 90 ns (shaping time=2 μ s). It is important to remember that the ASIC contains one more shaping time equal to 4 μ s, which in fact generates a longer delay than 90 ns.

Under these conditions, and in order to safely set a proper time to check the flag and avoid losing valid events, the longer delay must be taken as a global value. After including the internal flag delay plus external delays affecting the propagation of the signal, a safe time to check the flag status is about 6 clock cycles or 120ns after the clock edge.

7.2.7 Settling Time of Configuration Register

After the configuration register is modified, the ASIC has a settling time that must be respected in order to avoid reading out unreliable data. This is due to the fact that the baseline's stabilizer of each channel in the ASIC needs some time to settle down. Figure 48 shows the settling time simulation of one channel's baseline.

From figure 48 it is possible to estimate that the system is ready to start the acquisition phase after approximately 20ms. Even though this is a considerably big time compared to the period of the clock, the configuration process is usually done just once before starting using the device in a measurement.

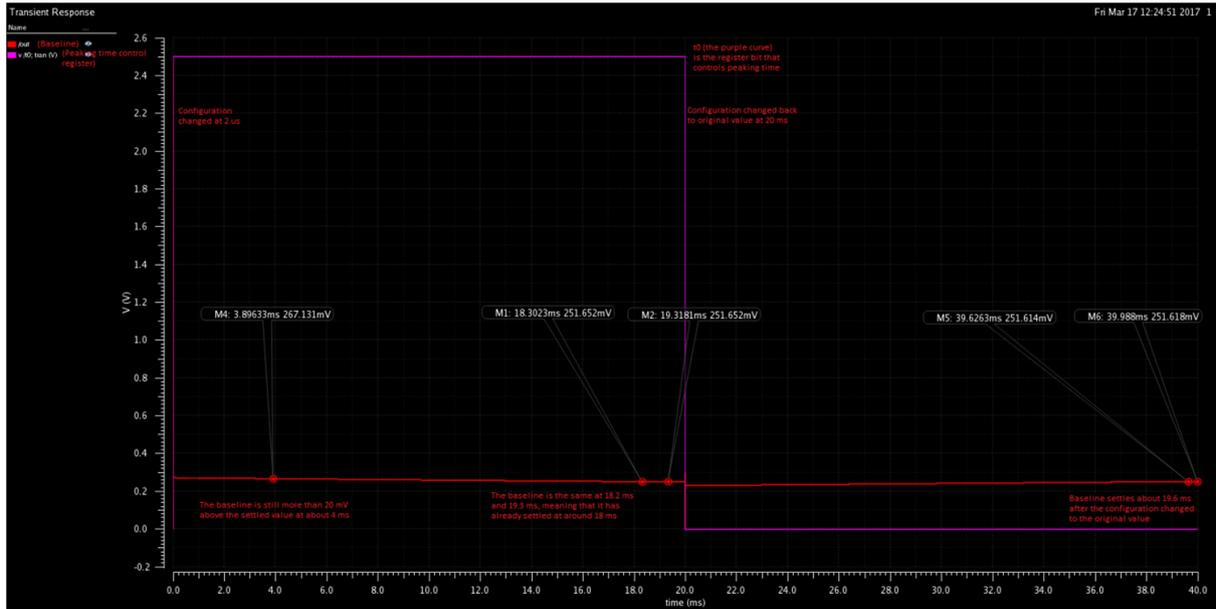


Figure 48. Settling time of baseline after configuration of the ASIC. Provided by Wenbin Hou – BNL.

8 First Hardware Version

8.1 Overview

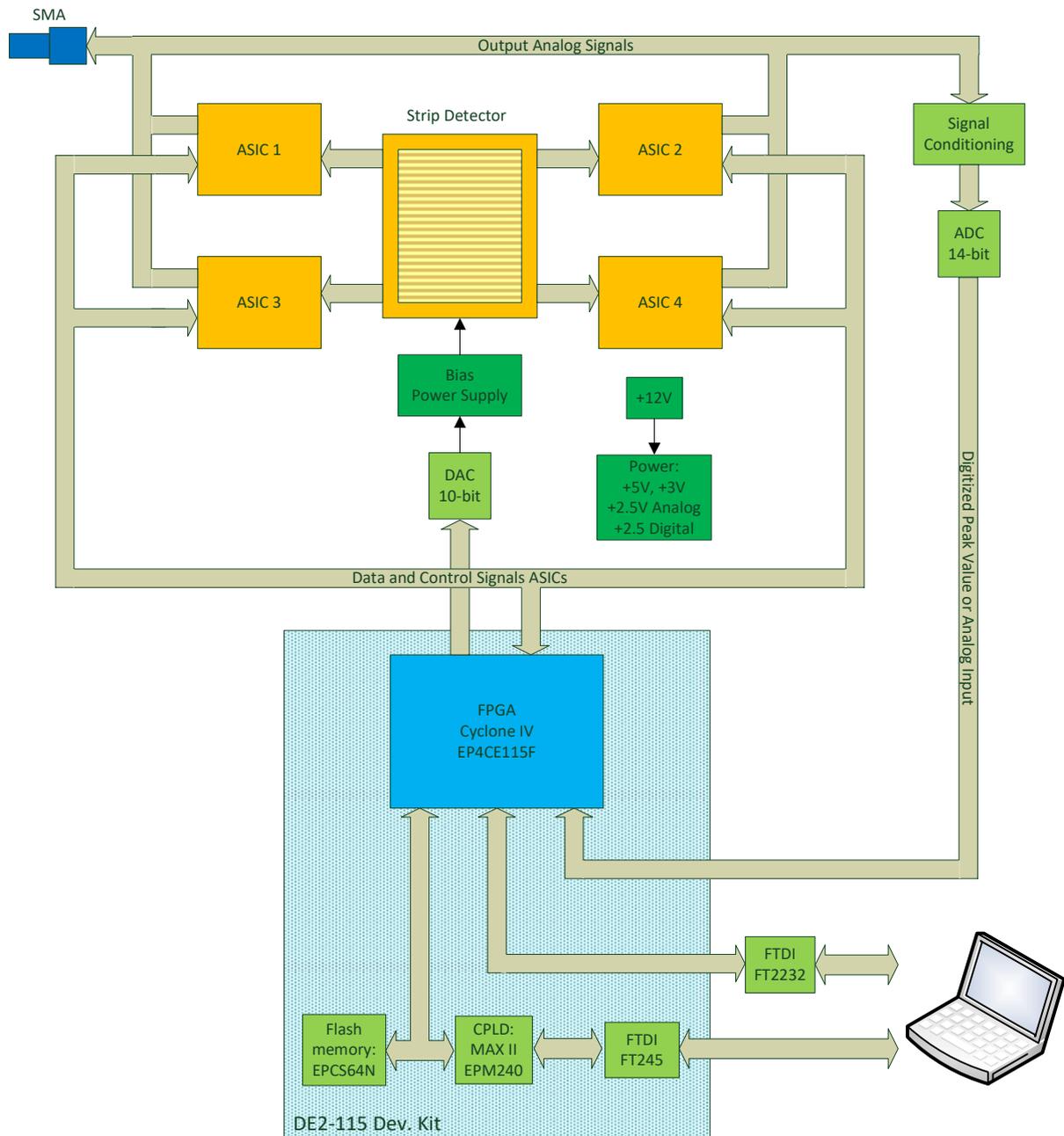


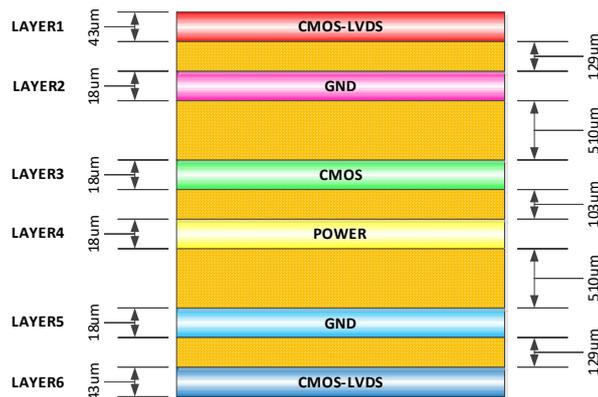
Figure 49. Block diagram of the first hardware version.

The first version of the design consists basically of one strip detector with 128 channels, 4 ASICs (32 channels each) packaged in 80-pin QFP cases, one fast ADC to digitize the analog signals, in-system bias voltage circuit to deplete the sensor and controlled by a serial DAC, an ALTERA FPGA development kit, a signal conditioning circuit, power supplies for all the components of the system, and components to interface the system with an external PC, as shown in figure 49.

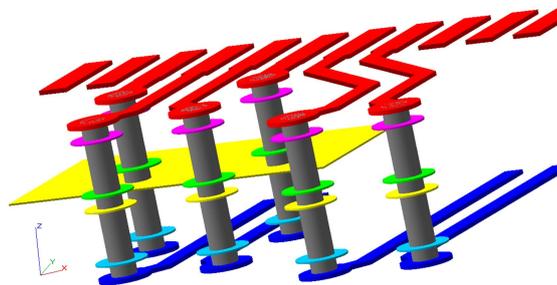
The FPGA works as the “brain” of the system; it controls the communication between the device and external computer, and according to the orders received from the GUI it fully drives the ASICs, sets bias voltage, executes automatic characterization routines and controls the A/D conversion of the analog signals.

8.2 PCB Design

The PCB was designed taking into account rules for systems mixing LDVS, CMOS and analog signals. The LVDS signals, as recommended, have a coupled impedance of 100Ω . The PCB has 6 layers and their distribution is shown in figure 50.



(a)



(b)

Figure 50. PCB layers. (a) Stackup, (b) detail of PCB traces.

As important as caring about mixing of signals, is the power supplies' noise. The power supplies were chosen because of their low noise level; however, it is really important to follow the layout recommendations given by the manufacturers in order to reduce the possible sources of noise and to improve the power dissipation. After soldering of the power supplies' components, tests were done with loads representing the real working conditions, as well as with loads representing much more exigent working conditions (higher load currents). In all the cases, the power supplies showed good performance.

Top and bottom sides of the PCB are shown in figure 51.

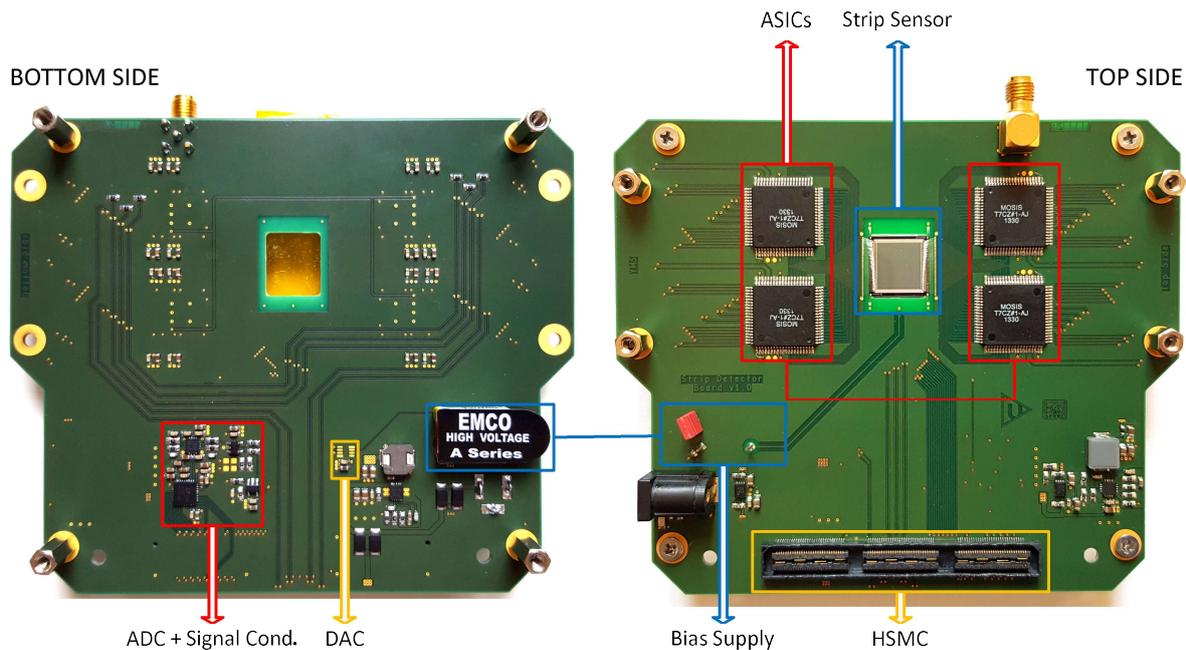


Figure 51. PCB sides: Bottom side (left), top side (right).

Figure 52 shows the complete assembled system.

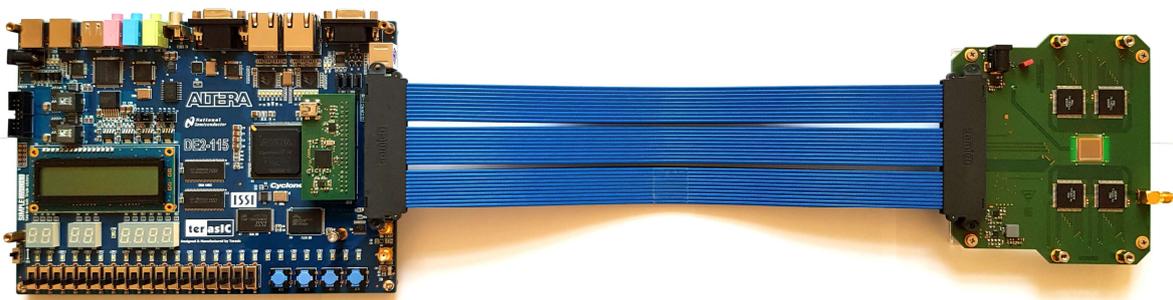


Figure 52. Complete system assembled.

In figure 52 it can be seen a high speed cable connecting the two parts of the system through the High Speed Mezzanine Card connectors (HSMC). This cable is used as a way of isolation of the ALTERA development kit from the radiation when the system is under testing in a radioactive environment.

8.3 Measurements

The measurements done with the first hardware version were mainly focused on testing of the functionality of the ASICs. For that, it is really important to fully understand the capabilities and properties of the ASIC, as well as its limitations.

As described in section 7.2, the ASICs have an internal test/calibration capacitor in each channel that let the designer to selectively test the channels. The test pulses can be controlled to inject a voltage peak with the wanted equivalent charge and polarity.

The first test was designed to verify the functionality of the control DACs. The first of them is the DAC controlling the amplitude of the voltage peak generated by the calibration capacitors. The output of this DAC can be verified after a 5:2 or a 5:1 internal voltage divider at the analog output pin OA. The results of the test can be seen in figures 53 and 54.

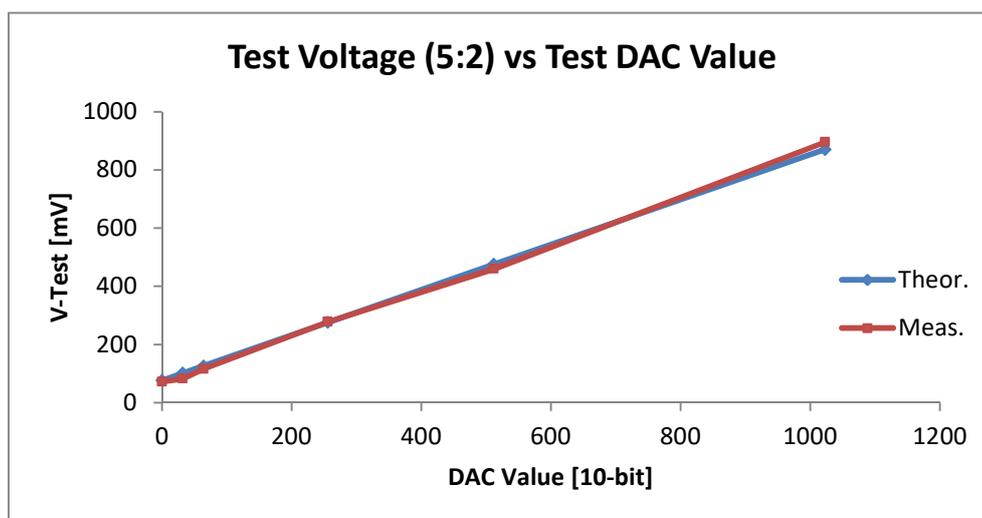


Figure 53. Peak amplitude of the test voltage after 5:2 divider vs DAC value; Theoretical (blue) and measured (red) values.

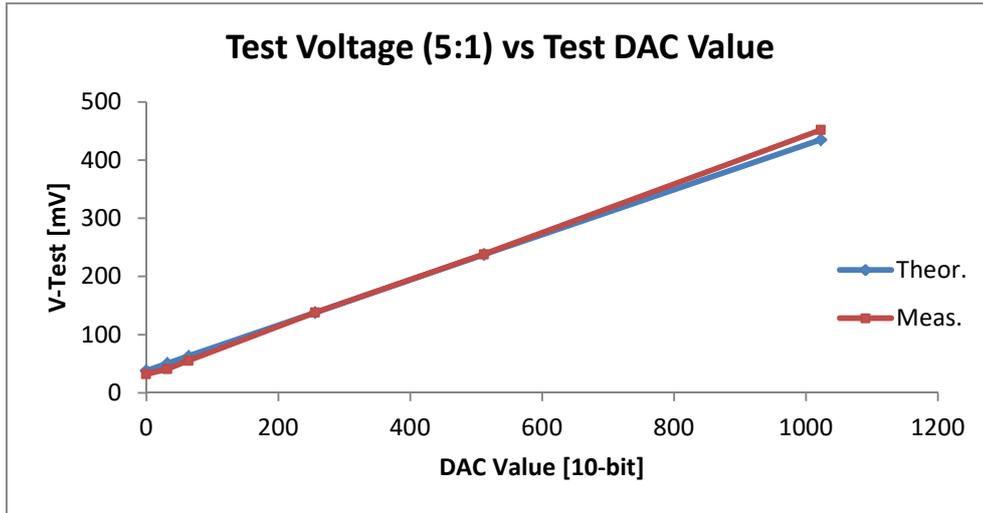


Figure 54. Peak amplitude of the test voltage after 5:1 divider vs DAC value; Theoretical (blue) and measured (red) values.

From figures 53 and 54, it is possible to see that the measured and theoretical values are in good agreement in this particular ASIC. A deeper analysis of the test pulse DAC will be provided in section 12, based on the second hardware version and for several ASICs.

The second DAC tested was the DAC controlling the threshold level. This DAC is very important since it is used during measuring to select the events' minimum energy level to be considered as valid, hence, removing noise and non-interesting events during measurements.

Figure 55 shows the result of the test.

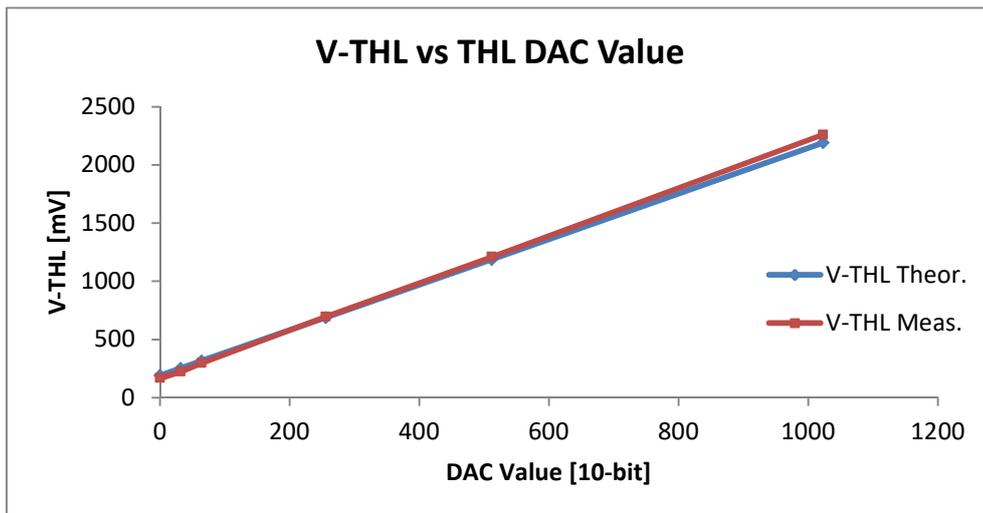


Figure 55. Threshold level vs DAC value; Theoretical (blue) and measured (red) values.

According to the results shown in figure 55, once again, there is a good agreement between the theoretical and the measured values.

A second test was implemented to compare the performance of every channel in two of the ASICs when applying the same input charge. Figure 56 shows the result of the test.

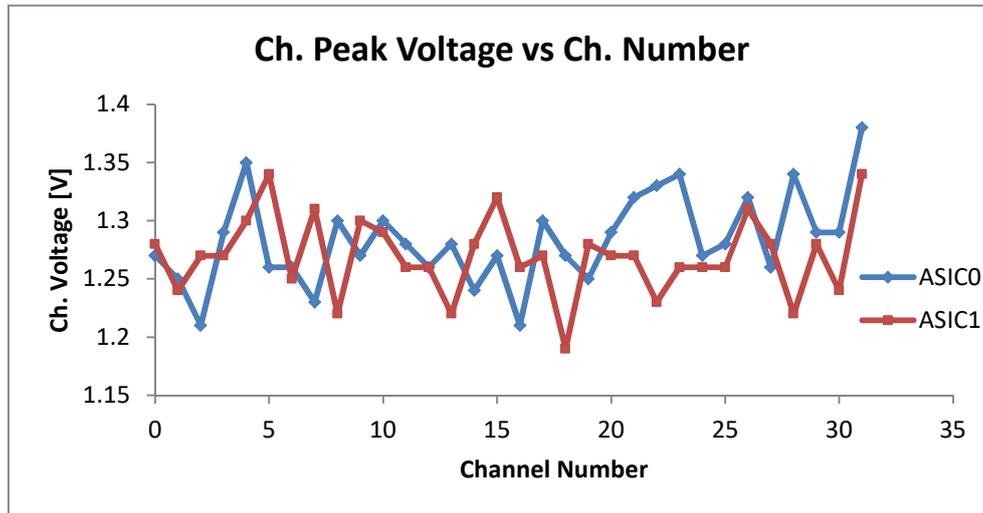


Figure 56. Peak voltage per channel for two ASICs (baseline subtracted), using a channel gain of 28.5 mV/fC and applying a charge of about 47.5 fC.

From figure 56 it can be seen that all the channels have slightly different performance when interacting with the same energy. This is a common behaviour in readout chips since the fabrication process is not totally perfect due to technological reasons. The same effect is possible to see in semiconductor sensors. No matter how precise the fabrication method is, every strip or pixel has a slightly different performance. However, this is not a problem; after connecting the strip sensor to the ASICs, all the system's channels can be equalized and calibrated to behave almost in the same way, having a more homogenous performance of the system.

The third performed test was focused on the ASIC's peaking times. The results of the test are shown in Figure 57. Here it is evident that the signals are lying on a DC level of about 250mV; this is the baseline implemented in every channel in order to keep the amplifiers in the high gain region. A deeper analysis of the baseline value is provided in later sections.

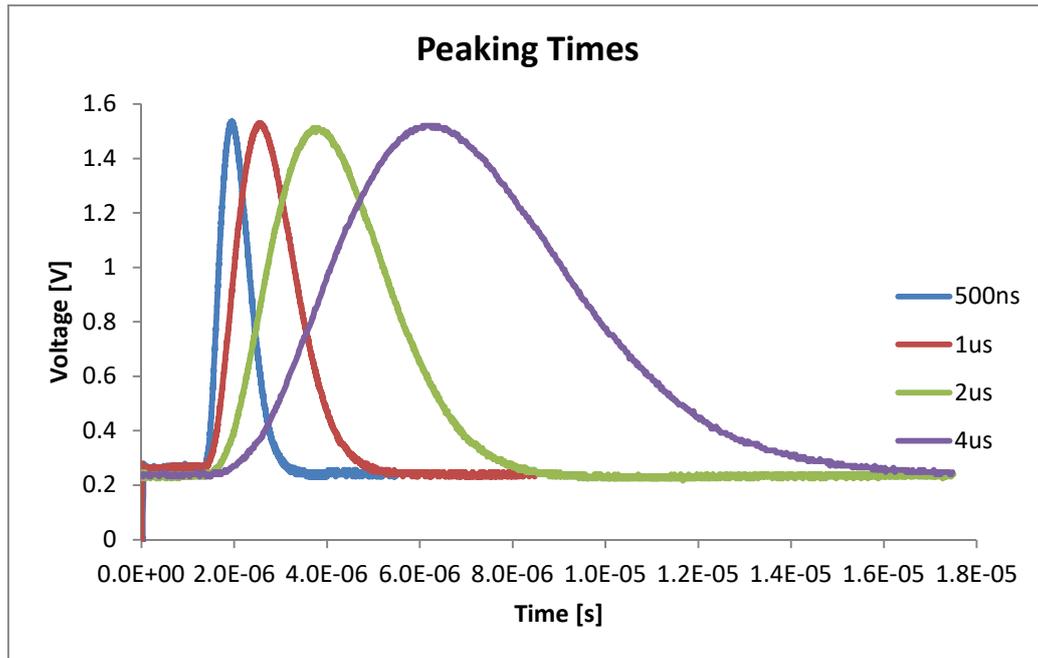


Figure 57. Measured peaking times for one channel.

The peaking time is another very important parameter because it influences directly the maximum speed of the readout process. Although short peaking times increase considerably the speed of the readout process, long peaking times have better Equivalent Noise Charge ENC when not affected by external sources of noise, e.g. noise coming from the sensor leakage current or from the bias supply [15]. This effect is more evident when the strip capacitances are higher. In the case of the strip sensor used in this thesis, the strip capacitance is small and there won't be big noise differences among peaking times.

9 Second Hardware Version

The first version of the system was a very useful tool to get familiar with the ASICs and understanding their behaviour. Additionally, it helped in the design of the firmware which drives the ASICs, controls the communication with the computer, among others. However, the first version is limited by its physical dimensions, number of lines connecting the constituent parts (mainly the HSMC connector), number of USB cables (x2) and external power supplies (x2). Additionally, it is clear that interconnection of the parts by wires means more noise added to the system.

Since this system is a mixed signal design, it is a must to reduce the Electro Magnetic Interference EMI produced by the digital signals because it distorts the analog signals containing very important and sensitive information. The best way to counteract this situation is carefully designing a single PCB layout containing all the components and reducing the size and number of external connections of the system; That is the main goal of the second version of the hardware. At the same time, smaller size means a device easier to use in real measurements and less sensitive to external interference. Additionally, some important extra features were included in the new version, making it more versatile and complete for future analysis and measurements. Figure 58 shows the second hardware version while figure 59 shows a comparison of the two hardware versions.



Figure 58. Second hardware version. It contains all the components in a single PCB.

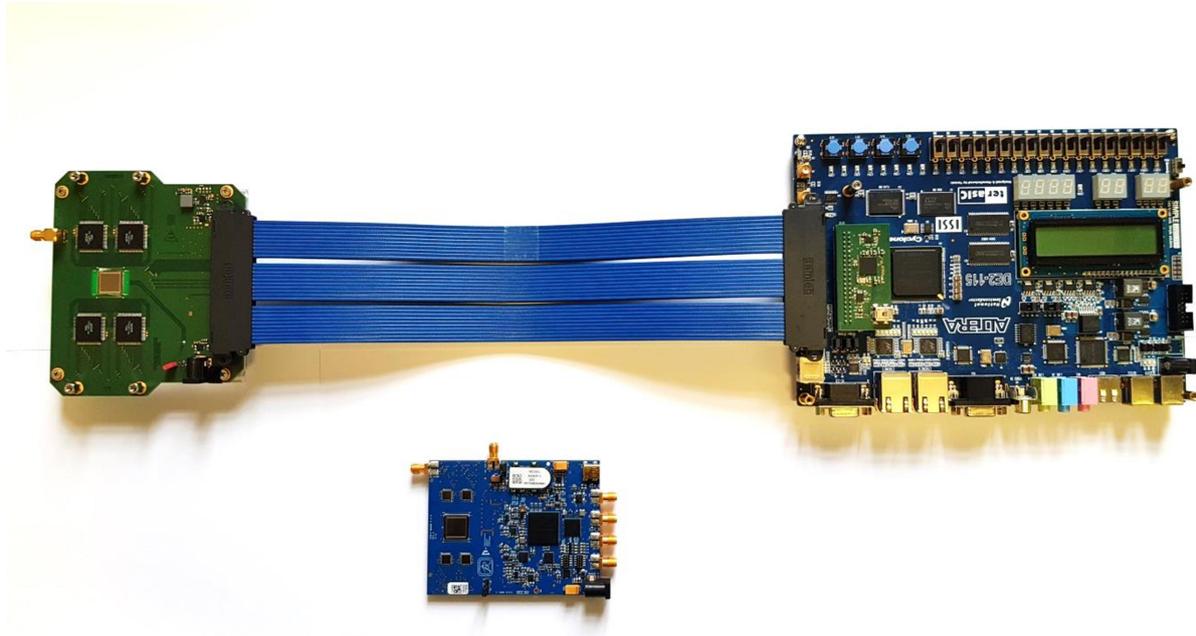
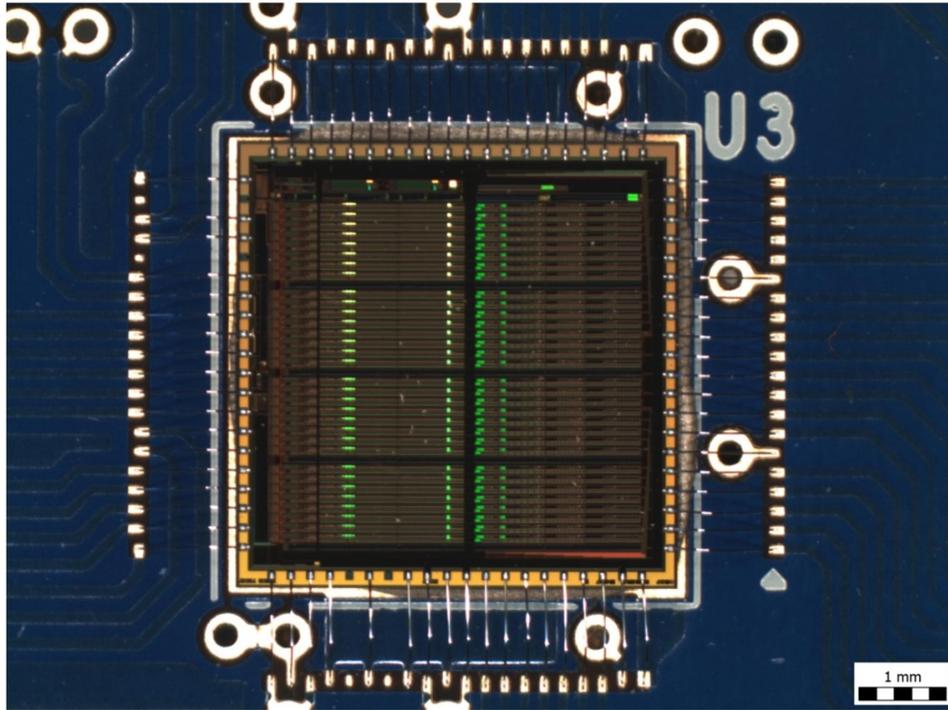


Figure 59. Size comparison of the two hardware versions developed.

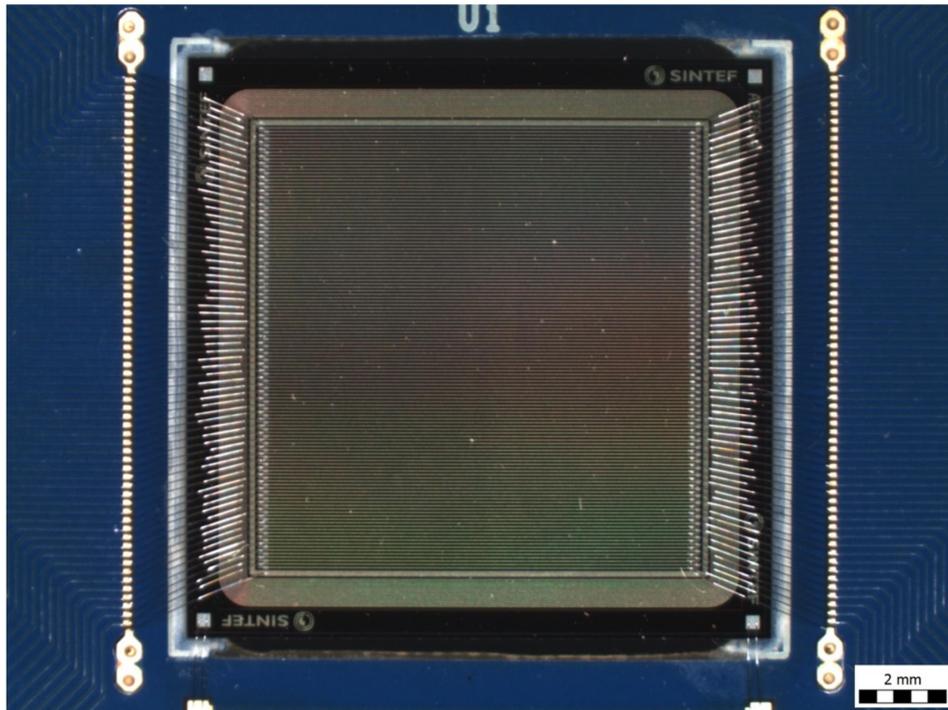
9.1 Overview

The second version of the design is roughly based on the first version; the main components contained in the first version are included; it uses the same strip sensor (128-strip), however, in the case of the ASICs and in order to minimize the PCB area, bare ASICs were used instead of the packaged versions. As it is clear, the connection of the ASIC's pins to the PCB traces was not done by soldering the pins (as in the first version) but by means of wire-bonds, similarly to the connection of the strip sensor's channels to the PCB. As in the first version, 4 ASICs are used to cover all the 128 strips.

Figure 59 shows a detail of the wire-bonds connecting the ASICs and strip channels to the PCB traces.



(a)



(b)

Figure 59. (a) ASIC's wire-bonds, (b) strip sensor's wire-bonds.

The extra features offered in the second version include a temperature sensor, dedicated I/O sma connectors for external clocks, I/O sma connectors for trigger signals, switch for int/ext bias supply, switch for analog signals, and Back Side Pulse Circuit. The I/O trigger signals can be used to create a system based on several devices in coincidence, e.g. a Time to Digital Converter TDC can be used to create a telescope. Figure 61 shows an sketch of the system.

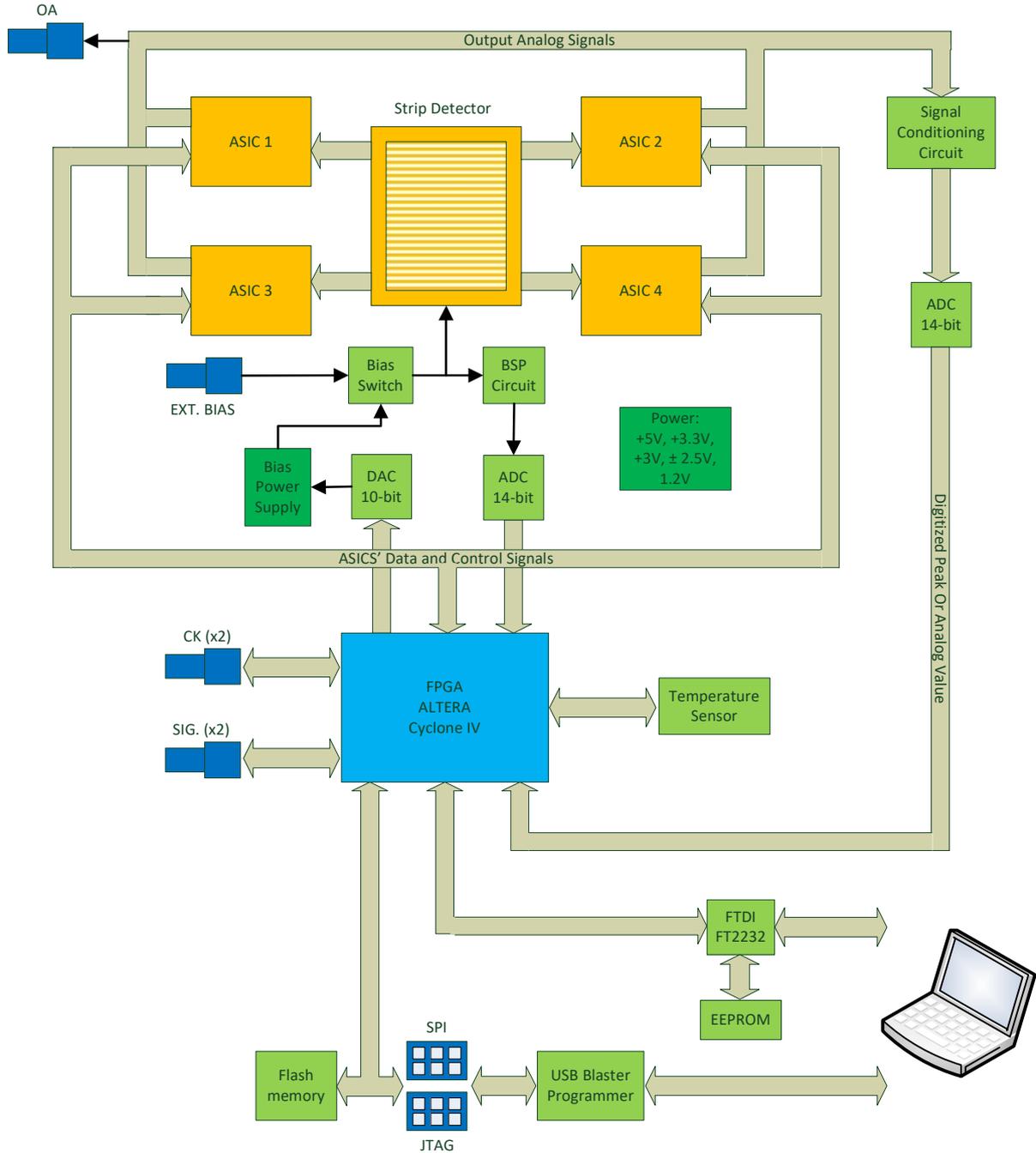


Figure 61. Block diagram of the second hardware version.

9.2 PCB Design

During the design of the second PCB version careful attention was paid to minimize as much as possible the noise levels and the PCB area. This is a complex task because the smaller the area the higher the signal interference and hence the noise.

When designing PCBs for systems containing analog and digital signals, or better known as mixed-signal designs it is easy to distort sensitive analog signals by surrounding digital ones or even cause interference among digital signals if the PCB layout is not designed carefully. The situation is even worse if the design is a High Density Interconnect HDI PCB because the signal traces and components will be much closer to each other and hence the possibilities of electromagnetic interference are higher.

In order to minimize the noise of the system, several points were taken into account in the second version: The first point is to avoid the destructive influence of the single ended signals on the differential signals. For that it is necessary to follow the recommended physical separation between these two types of digital signals when placed on the same layer.

The second point is to avoid the noise contribution of any type of digital signal on the analog signals. As in the previous point, the correct separation plus correct grounding clearly improve the results. This is especially important in this design considering the fact that the analog signal delivered by the ASICs corresponds to the energy measured by the channels; any distortion of the analog signals means worse energy resolution of the system or even the limitation to measure low energy values.

A third point is the need of using independent power supplies for the digital and for the analog parts of the circuit, even if they have the same value and polarity. The noise produced by the fast transitions in the digital circuitry can easily be fed to the analog circuits due to the fact of having a common power supply.

The last point, usually not taken into account, is the separation of the analog and digital grounds. This point is very important because only following the first three points and forgetting about the correct grounding will be useless in terms of effectively reducing the noise levels. This is probably the most difficult part of the PCB design, because it needs a good understanding of the ground return currents according to frequency of the source and to the position of the components.

9.3 Measurements

In order to test the new hardware version, two different measurements were performed. The first one was the measurement of internal test pulses. This is an easy way to compare the performance of every channel in the system because external devices or radiation sources are not needed. Several tests were carried out, each for a different pulse amplitude. The method consists in applying the same pulse amplitude to all the system's channels and the output signal is digitized and sent to the computer to be compared with its theoretical value. Figure 62 shows that the output signal of each channel is slightly different, but the differences are smaller when the channels belong to the same ASIC.

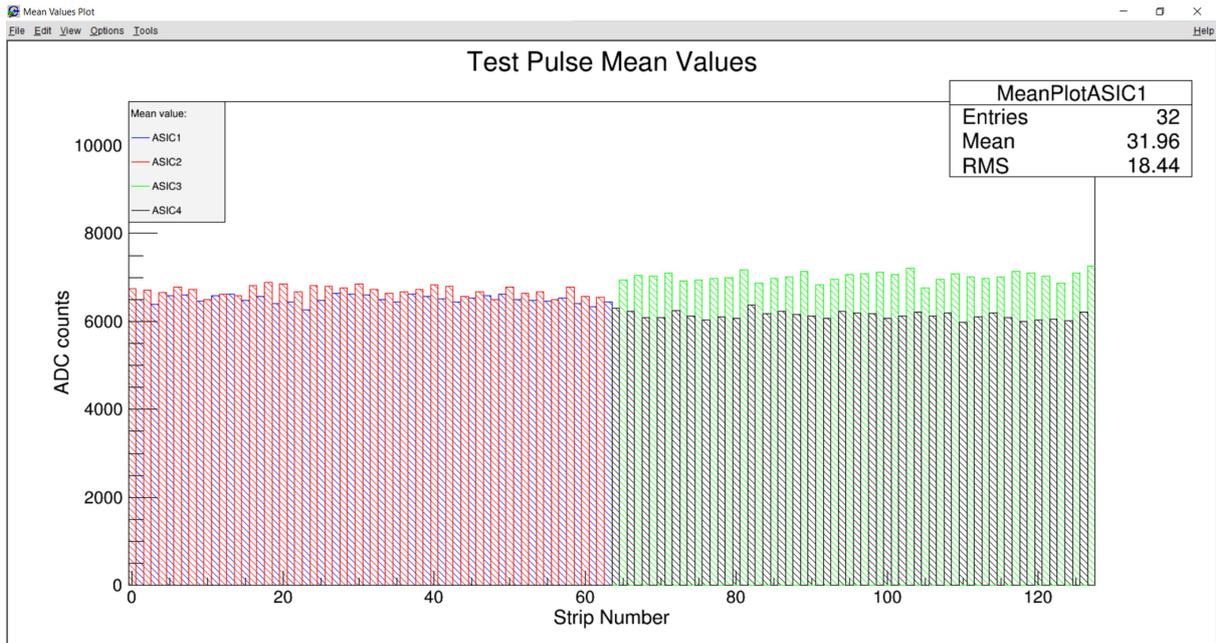


Figure 62. Test pulse mean value after 1,000 pulses were applied to each channel. Gain=57mV/fC, shaping time=500ns, Test DAC=128.

The second measurement was used to verify the differences in performance shown in figure 62. The idea was to measure a mono energetic source of radiation not affected by the interaction with air. The selected radiation source was gamma photons from 241Am. Figure 63 shows the result of the tests.

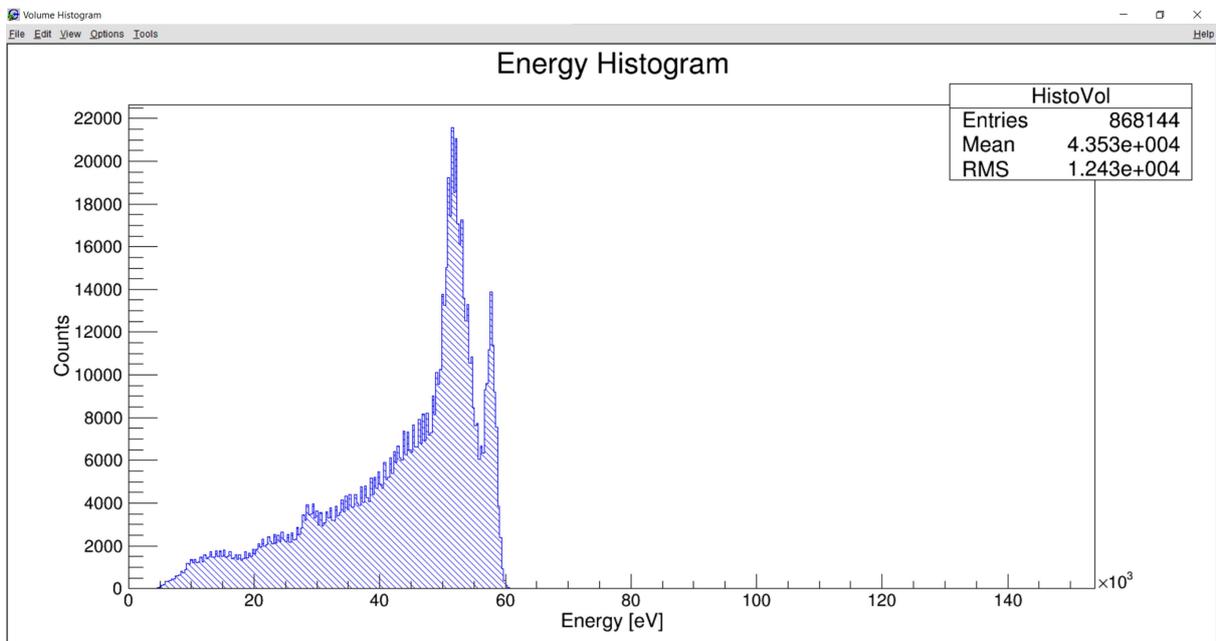


Figure 63. Measured energy spectrum of 241-Am gamma photons (no calibration).

This measurement differs from the previous one because the measured energy comes from the charge deposited by particles in the strip sensor and not from the ASIC's internal test capacitors.

From figure 63 it is visible that two peaks are produced for the same mono-energetic source, evidencing the different performance of the ASICs and channels noticed in the previous test. Even though the system is composed of 4 independent ASICs, their ideal performance together should produce a single peak. Additionally, another important aspect that can increase the differences channel to channel is the baseline value. The baseline should be theoretically equal to 250mV, but in reality it has a slightly different value for each channel. Figure 64 shows a scan of 4 baseline values of the system.

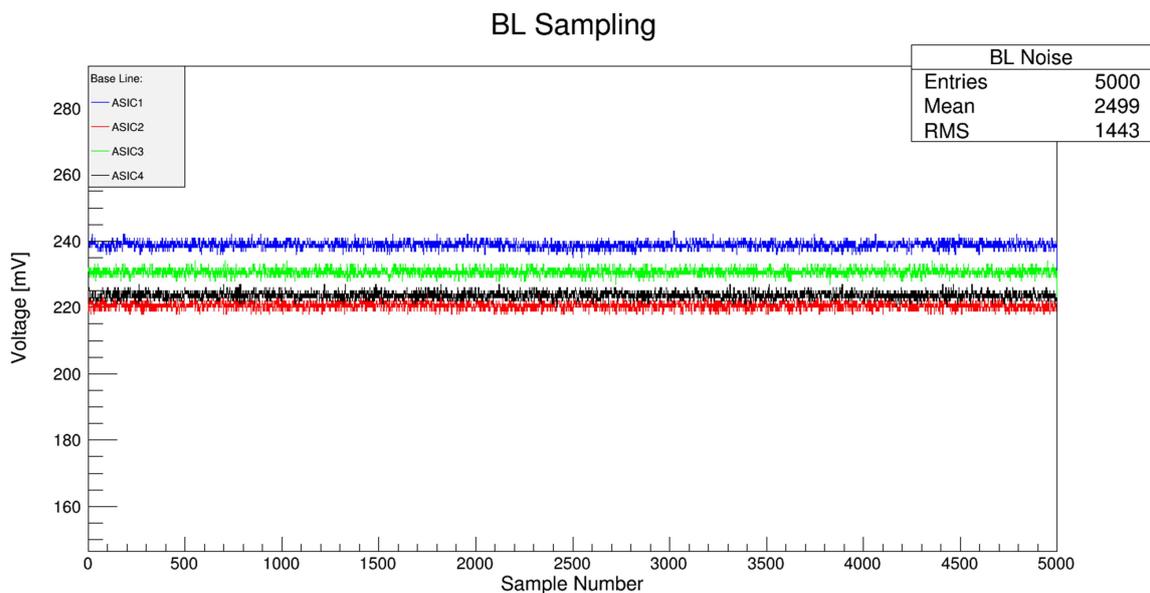


Figure 64. Baseline sampling for channel 10 in all four ASICs.

Since the real analog output value of the ASICs is calculated as the difference between the PD output value and its corresponding channel's baseline, the fact that each ASIC or even each channel has a slightly different baseline means that channel to channel differences are more evident and hence more than one peak appear when measuring a mono-energetic source of radiation.

In order to counteract these and other effects produced by the unique performance of each channel (common situation in any semiconductor detector), the system must undergo fundamental equalization and calibration processes before using it in any application. Sections 12 to 14 explain these processes more in detail.

10 Firmware

The system contains two clock domains: The first one is 50MHz which corresponds to the ASIC's maximum recommended clock frequency. The second one is the associated 60MHz clock for a synchronous communication through the FTDI chip (USB). The firmware was designed to cope with this two clock domains and to interface them during data transfer. Additionally, an extra clock of 100 MHz is derived from the 50 MHz clock to feed the BSP circuit.

Even though the clock frequency of the ASIC is 50MHz, the readout process doesn't read the channels' information every 20ns. This is because two important signals have delays which are bigger than the clock period. These two signals are the peak detector PD and the readout flag FL.

As mentioned earlier, the PD pin outputs the analog values saved in the ASIC's analog memory. The time delay of the transition from the previously read value to the new one varies depending on their difference in voltage. In that case, it is necessary to consider the worst case: the PD signal makes the maximum excursion (2V). Moreover, the signal takes an additional time to settle and this must be included during the readout phase. Figure 65 shows a sketch of the PD signal behaviour.

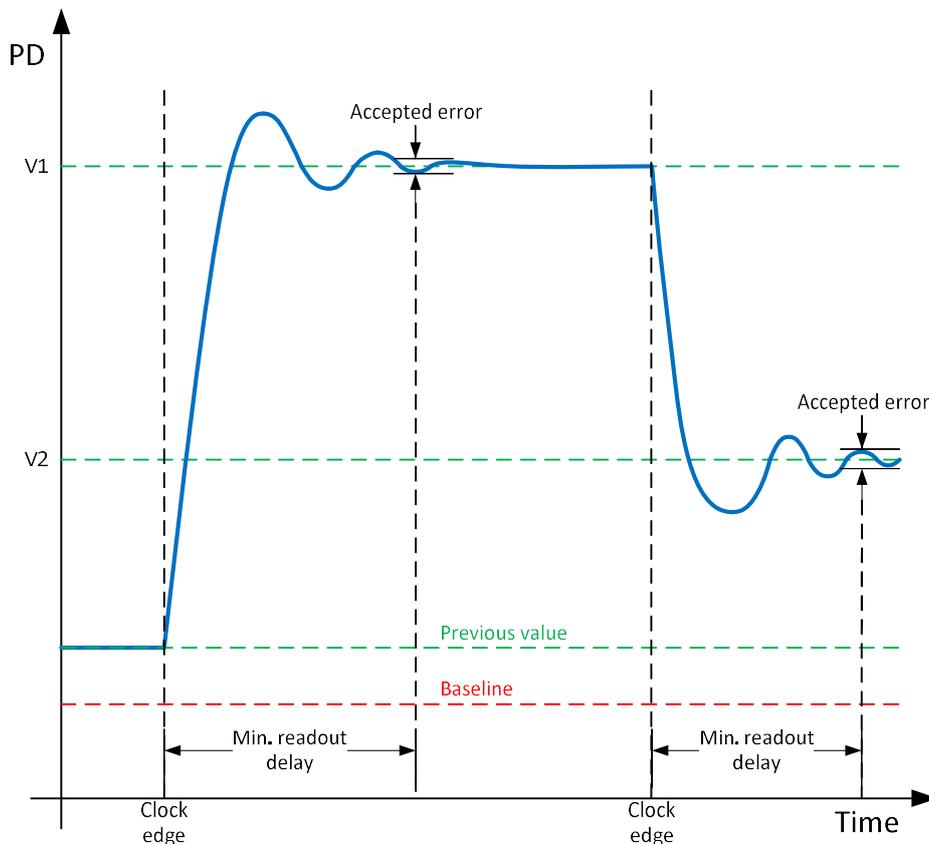


Figure 65. PD signal behaviour during readout phase.

As seen in figure 65, when a clock edge is detected during the readout phase, the PD signal changes from its current value to the next value from the analog memory. Then the signal has an overshoot followed by a ringing; hence the correct time to sample and digitize the signal must be set accordingly. The sampling time must give the signal the possibility to be within an accepted error from the goal value; shorter time affects the energy resolution while longer time increases the dead time of the readout process. The sampling time and simulation of the PD signal were previously shown in figure 41.

Regarding the readout flag, as in the case of the PD signal, it has a delay which is bigger than the clock period. During the acquisition phase, the readout flag is set every time there is at least one valid event available. During the readout phase, a clock pulse is applied to output each available value recorded in the analog memory. If a clock pulse lowers the readout flag, it means that the last read value was the last available. A simulation of the flag delay to lower is shown in figure 66.



Figure 66. Simulation of the flag delay after clock edge to lower. Provided by Wenbin Hou – BNL.

Even though the PD signal and the readout Flag are triggered by the same clock edge, the readout flag signal goes directly to the FPGA while the PD signal is additionally delayed by the signal conditioning circuit. During the readout phase the flag signal is monitored in order to detect the end of available data; if the flag doesn't lower after the appropriate waiting time means that there is a new analog value to read and the waiting time must be prolonged in order to give the PD analog signal the chance to settle. Taking into account all the delays and in order to have a good resolution in the system, a safe sampling period of the PD signal was set as 13 clock cycles (260ns), as shown in figure 67.

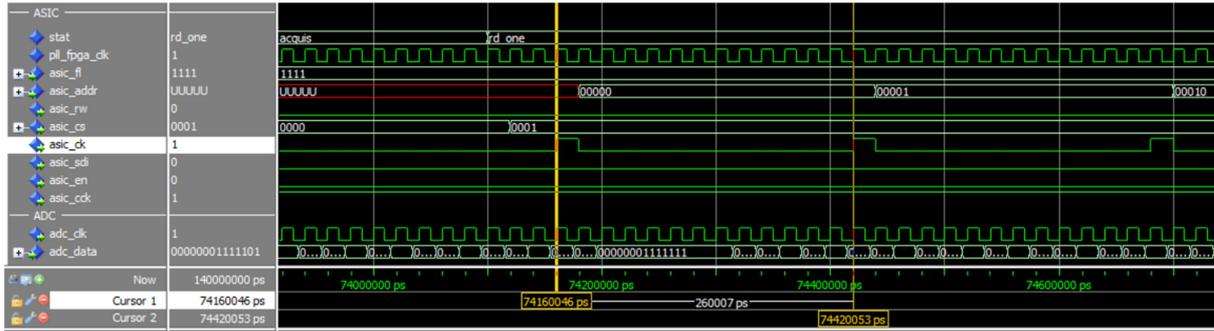


Figure 67. Readout period.

There is an additional delay to take into account in the firmware, and previously described in section 7.2; this is the assertion delay of the readout flag. It doesn't affect the readout phase but slightly increases the dead time of the system. Once a valid event is detected by at least one of the peak detectors in the ASIC, there is a delay until the flag pin goes up. In order to make the firmware as simple as possible, the maximum delay value (for shaping time=4 μs) was considered in the firmware.

Since the data taking process includes delays and waiting times from the acquisition and readout modes, and with the aim to make it more understandable, figure 68 summarises the whole data taking process.

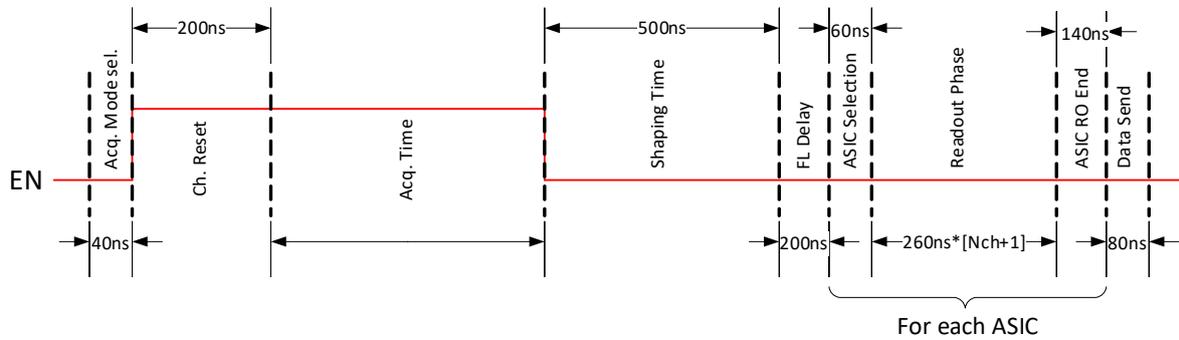


Figure 68. Time diagram of a complete measurement (acquisition + readout) when using shaping time =500ns.

From figure 68 the readout period of a complete frame can be expressed as:

$$T = 1020ns + AcqTime + \sum_{i=1}^4 [260ns * (nCh_{ASIC_i} + 1) + 200ns] \quad (6)$$

Using equation 6 it is possible to calculate the maximum data rate, supposing the atypical situation when all the channels in all four ASICs have a valid event; this provides a data rate of 36,140 frames per second. This data rate can also be expressed as 14.1671 Mega Bytes per

second, which is managed without problem by the synchronous configuration of the FTDI device (up to 40MB/s).

Regarding the communication between the device and PC, a simple but functional protocol was developed. The information read from the ASICs, temperature sensor, or Back Side Pulse circuit is sent to the control PC through 4-Byte “bursts”. If the information is about data read from the ASICs, each burst sends information about one single channel. In the case of handling temperature or BSP data, the burst contains information about a single sampling of the system’s temperature or BSP, respectively. Figure 69 shows a brief description of the communication protocol.

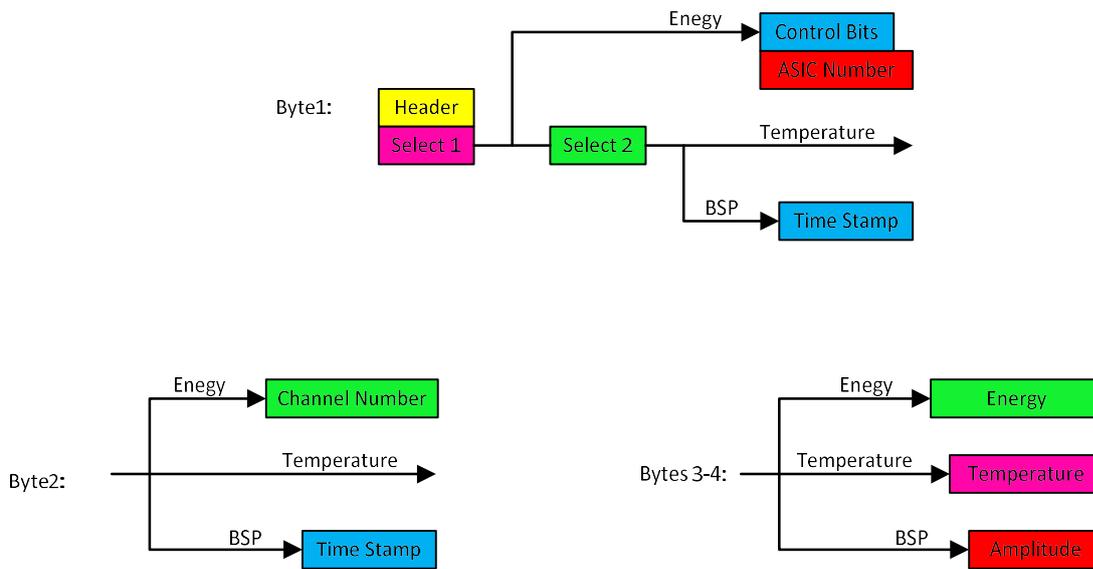


Figure 69. Block diagram of the Device to PC communication protocol.

11 Software

A custom designed software was developed to drive the strip sensor-based system. The software permits to use the devices in real measurements, and at the same time it has available all the necessary routines to fully characterize the system. The software name is StripPlus and was developed in C-sharp (C#). Figure 70 shows the software GUI.

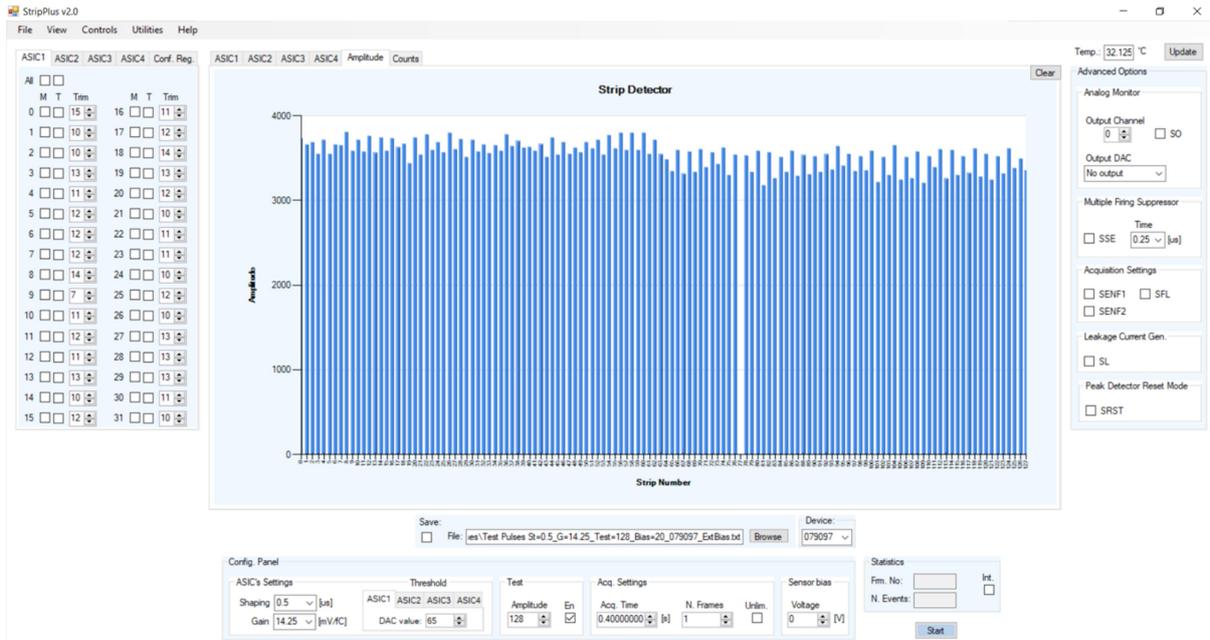


Figure 70. StripPlus graphical user interface GUI. Measurement of test pulses is shown.

The GUI has three different types of graphs: one type (ASIC1 to ASIC4 graphs) shows the amplitude of the events recorded by the channels of each ASIC independently; a second type shows the amplitude of the events of all the channels of the system in their real position on the sensor; and a third type shows the counting mode of the previous type.

The software provides options to save and load configuration files; Each device has two configuration files: one (Trim File) contains all the information about the equalization of all the system's channels and the second one (Config File) contains information about threshold values, shaping time, gain, acquisition time, bias voltage (in-system circuit), test voltages, and other important parameters of the ASICs. Before starting any measurement both files must be loaded to the software. All the loaded values are displayed and can be modified according to the needs. Additionally, the software sets default values for all the parameters of the ASICs, making the system ready for standard measurements. If needed, advanced parameters can be manually changed for special purposes.

There are three characterization functions implemented in the software: Threshold DAC Scan, Test DAC Scan, and Baseline Scan. These functions use part of the advanced parameters of the ASIC but after finishing the values are returned to their defaults. The

threshold and test DAC scans provide data sampling of every step of the DACs which is important to calculate their real baseline value, as well as their linearity. In the case of the baseline scan, it provides vital information about the baseline of each channel of the system. This information is primordial in the calibration and energy calculation during postprocessing.

After the baseline scan function has been run, the calibration procedure can start. There are two methods of calibration available in the software: one is the calibration function based on the internal test pulses. Basically, it applies 1000 pulses with the same amplitude to each channel and saves the output data in a file. This procedure can be repeated for different amplitudes, hence having several energy points to fit a calibration curve for each channel. Since the test pulse circuit of every ASIC is slightly different, it must be characterised very deeply, and consequently this method is used mainly as an approximation (explained more in detail in the calibration section).

The second method is based on standard measurement of events from radioactive sources with well defined energy (mono-energetic). The measurement is done for several energy peaks independently and the result is a custom calibration curve for each channel.

It is important to say that the software is designed to display and save data in particular formats according to the used function. Postprocessing and data analysis was done by additional C++ and ROOT (CERN) scripts not included in the software. The postprocessing includes routines performing pattern recognition, custom fitting functions, statistics, custom graphs, etc.

Additionally, the software provides the possibility to measure and display the temperature of the device. This is important in order to monitor the temperature of the sensor and ASICs during any measurement. Moreover, an integral mode of visualization can be activated with the purpose of seeing the distribution of events during certain period of time.

Regarding the communication PC-device, it is similar to the device-PC's structure but the length of the burst varies according the type of command. This is because each order must include different amount and type of information from the GUI.

Figure 71 shows the data sets used for the different control functions.

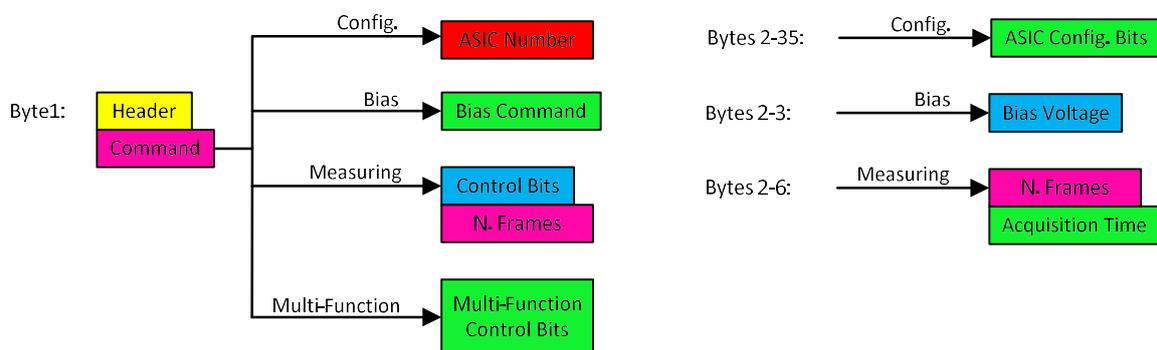


Figure 71. Block diagram of the PC to Device communication protocol.

12 Baseline Scan

Even though photolithographic and chemical processes involved in the fabrication of ASICs is nowadays at a very advanced stage, the fabrication of front-end electronics for semiconductor sensors is still not perfect. All the channels of a particular ASIC are designed to be equal, however, in reality the performance and voltages are slightly different channel to channel, and even more ASIC to ASIC. This affects notably systems containing multiple ASICs which aim to increase the number of channels in order to cover bigger areas. These differences channel to channel decrease the resolution of the system and make data analysis more difficult when close energy peaks are to be measured.

The baseline scan is the first step in the characterization of the system, and in order to minimize the situation previously described, it must be executed for all the channels in all the ASICs. The baseline scan is an extremely important and basic process that must be performed to obtain crucial information of the channels, later used in the equalization and calibration processes, as well as in the energy calculation.

In the ASIC, every channel contains a baseline voltage on which all the incoming signals are referenced to, so this value must be well known. This value is theoretically constant (250mV), however, as explained before, there can be differences in its value channel to channel or even more ASIC to ASIC. The baseline voltage of each channel is produced in combination between the global voltage produced at the bandgap reference circuit and the loop created by baseline stabilizer and the shaper of each channel [9], [17]. Eventhough the baseline stabilizer and the shaper of all the channels are once again designed to be equal, there are small mismatches in the transistors which produce slightly different baseline values. The baselines are included in the ASIC in order to keep a high open loop gain in the internal OpAmps used in each channel. The OpAmps are a key part in processing of the analog signals coming from the sensor.

The baseline scan process starts by doing a rigorous scanning of the baseline voltages of every channel in all the four ASICs of the system. Since the baseline voltage is affected by different inherent noise sources (previously described in the Noise Analysis section), the result of the scan will not provide a constant value but a distribution that can be modelled as a Gaussian, as shown in figure 72. From the Gaussian distribution two important values can be obtained: Baseline value (mean value) and noise level (standard deviation).

Once the two parameters are found for every channel in the system, a file containing this information is saved and must be used for any further characterization or data analysis.

The next step is to equalize the channels.

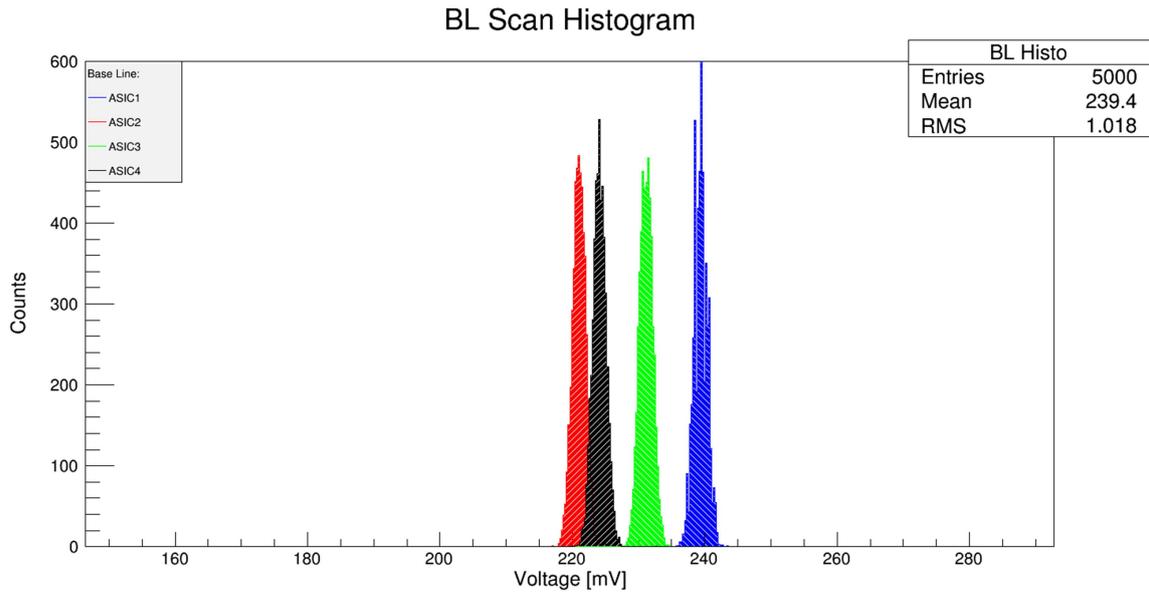


Figure 72. Noise distribution around the baseline of channel 10 in all four ASICs.

13 Equalization

The equalization process provides a tuning of the “sensitivity” of the channels, which means that the channels’ discriminators will be set to accept events with the same or similar minimum amount of energy. This is a process that is directly controlled by the position of the global threshold of the ASIC respect to baseline of every channel. The goal of the equalization consist in finding the minimum global threshold value that can be used taking into account that this value must be far enough from the noise level present in the system; this avoids fake events produced by the noise to be taken by the discriminators and recorded by the analog memory of the ASIC, but still being able to record events with as low energy as possible.

Since every channel has a slightly different baseline value, a global threshold value makes impossible to reach the same sensitivity in all channels. To avoid this situation, the ASIC includes a TRIM DAC in every channel (described in section 7.2). The purpose of the TRIM DAC is to independently modify the global threshold level coming to the channel’s discriminator.

The equalization starts by detecting the noisiest channel of the system, which means the channel with the highest standard deviation (σ) when counting all four ASICs. Even though every ASIC should be treated independently (having its own noisiest channel), it is more convenient in terms of noise to use the highest noise level of the whole system as a reference because all the ASICs are connected to a single strip sensor. The reason is that all the channels, independently from which ASIC they are, must be set to the same minimum energy sensitivity. Figure 73 shows an example of noise level for all the channels of the strip sensor.

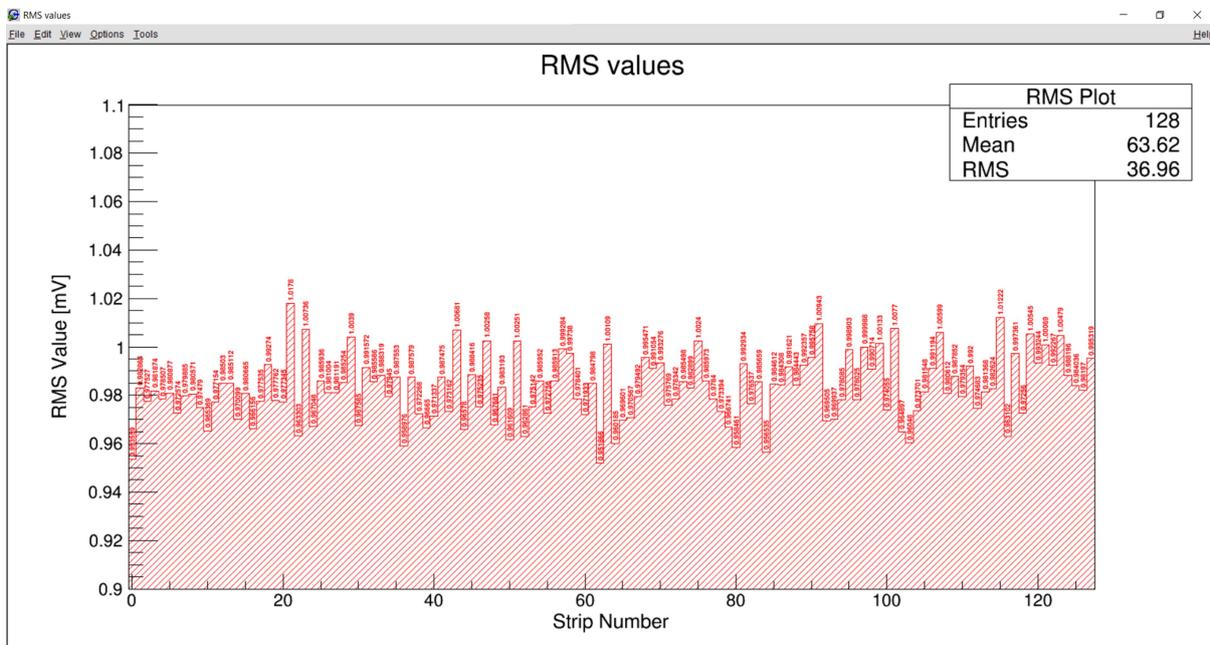


Figure 73. RMS values for all the strip channels. Noisiest channel=10, ASIC1, Strip=21.

At this point of the process, it is important to be careful when choosing the noisiest channel of the system because there can be damaged or too noisy channels that can substantially increase the minimum threshold value, hence increasing the minimum detectable energy of the whole system. To avoid that situation, a thorough analysis of the noise profile of the noisiest channels must be done. In case a channel has a too broad noise distribution, it must be discarded as the noise reference channel and instead it must be masked.

In order to be safely away from the noise, there are different approaches about how far from the noise mean value the threshold has to be; one option is for example 3σ which means that there is a 99.73% of probability to avoid taking noise events as real events. Another possibility, which is much more conservative, is to use 6σ leading to a 99.99% of probability to avoid noise events. In this thesis 6σ was used as the discrimination criteria; this produces a very clean spectrum but slightly decreases the sensitivity of the channels. Figure 74 shows an example of the procedure.

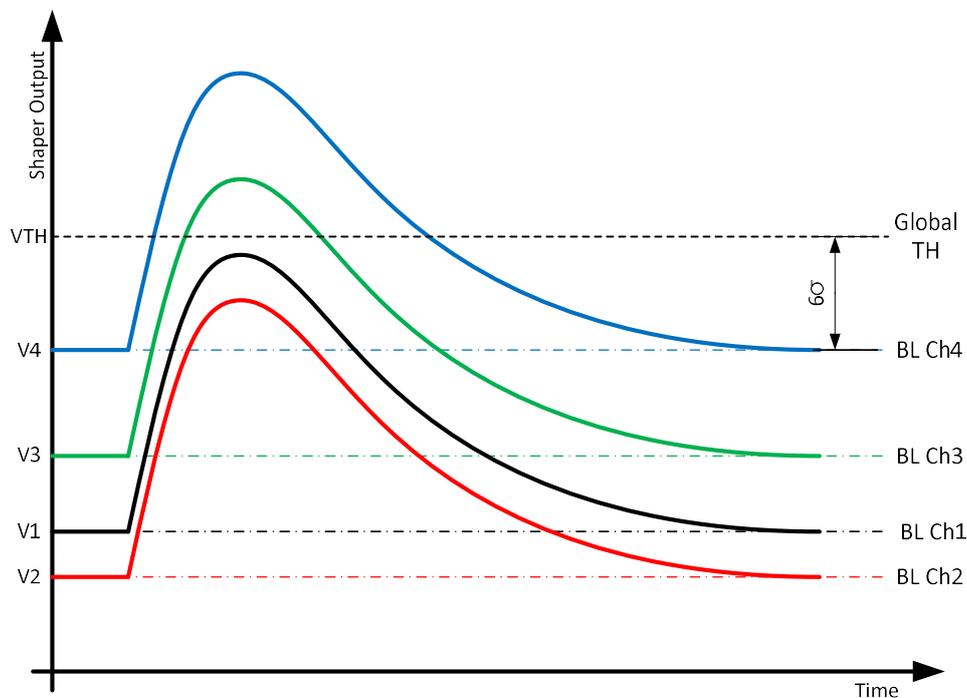


Figure 74. Example of the global threshold calculation (for four channels) during the equalization process.

As shown in figure 74, the threshold is placed at 6σ above the baseline of the channel with the highest noise level. This difference is a very important parameter because it provides the minimum amount of energy that the system will be able to measure; in other words, the real global sensitivity for every channel.

Once the 6σ value of the system is found, the equalization continues by calculating the global threshold value of each ASIC. Ideally, a single global threshold would be valid for all the

ASICs in the system, however, since the differences ASIC to ASIC can be higher than the range of the TRIM DACs, it is necessary to calculate an independent threshold for each one (opposite to the case of the standard deviation). As previously described in the section 7.2, the TRIM DAC is only able to decrease the global threshold value. In that case, the reference channel for the calculation of the global threshold must be the channel with the highest baseline. Knowing this, the global threshold of each ASIC can be calculated as the sum of its highest baseline plus 6σ .

Since all the channels of the system must have the same sensitivity, or at least very similar, the last part of the equalization consist of setting the threshold position independently for each channel (except for the reference channel of each ASIC) to the same 6σ distance from its own baseline value. This is accomplished by using the TRIM DACs of every channel. Using equation 5 it is possible to set this difference. An example of the result of the equalization process is shown in figure 75.

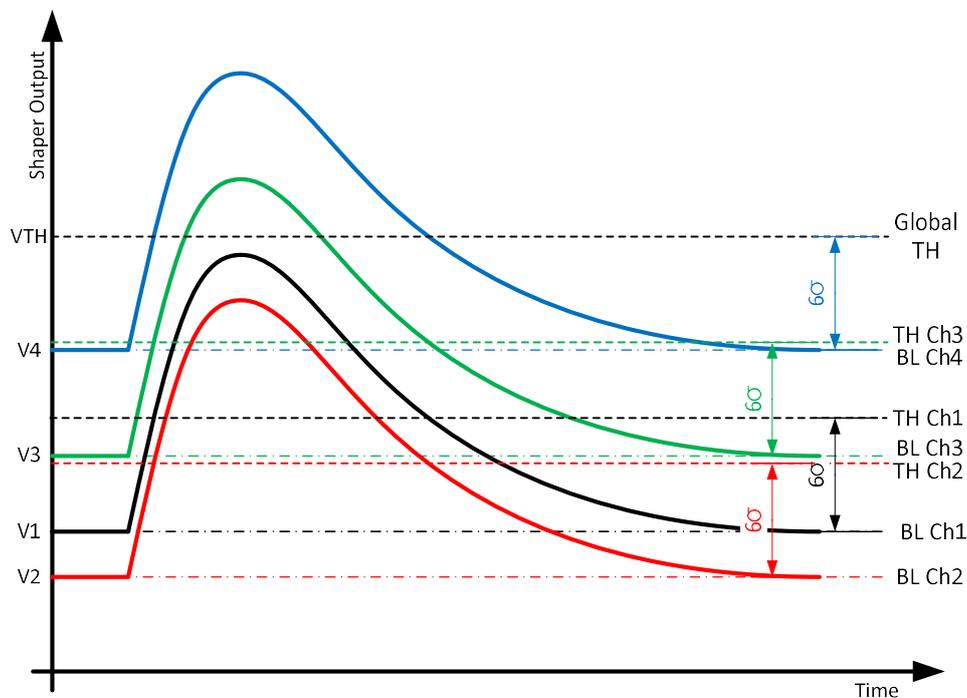


Figure 75. Example of the threshold equalization for four channels.

After the full equalization of the system was completed, the threshold value of the system was set to approximately 3 keV, which corresponds to the 6-sigma approach.

Finally, after the full description of the equalization process, a mathematical explanation of how to calculate the threshold DAC value when the system deals with a possible offset added by the signal conditioning circuit can be given. Figure 76 shows a sketch of this situation.

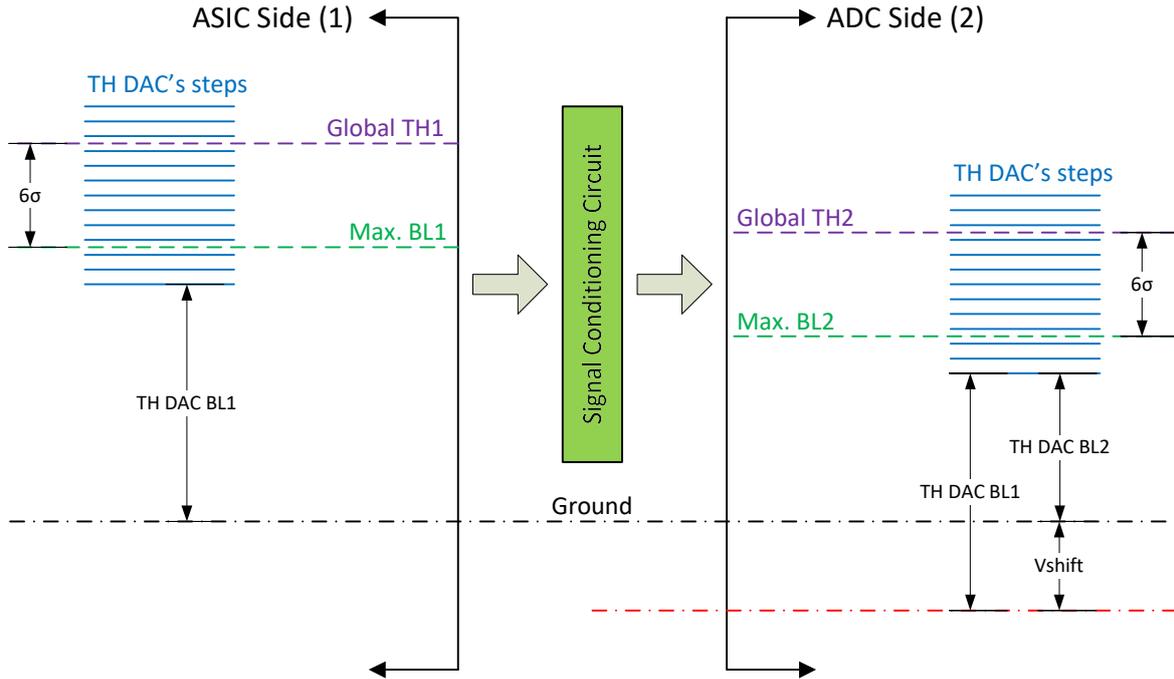


Figure 76. Analysis of the signal conditioning added offset.

From figure 76 the analysis below can be done, taking into account that when using the subscript 1 means before the signal conditioning circuit and subscript 2 means after, and the units are shown in brackets:

The 6σ value of the system is

$$SixSigma_{[counts]} = 6 * maxSigma_{sys[counts]} \quad (7)$$

where counts units refers to ADC counts. Then the global threshold value after the signal conditioning circuit is

$$GlobalTH_{2[mV]} = (maxBL_{2[counts]} + SixSigma_{[counts]}) * ADCstep_{[mV]} \quad (8)$$

Comparing the global threshold value before and after the signal conditioning circuit we can write

$$GlobalTH_{1[mV]} = GlobalTH_{2[mV]} + Vshift_{[mV]} \quad (9)$$

where V_{shift} represents positive or negative offset added to the signal. The value set for the threshold DAC can be express as

$$THDACPos_{1[DAC\ counts]} = (GlobalTH_{1[mV]} - THDACBL_{1[mV]})/THDACstep_{[mV]} \quad (10)$$

and the value of the threshold DAC's baseline as

$$THDACBL_{1[mV]} = (THDACBL_{2[counts]} * ADCstep_{[mV]}) + Vshift_{[mV]} \quad (11)$$

Combining the equations 8 to 11 we obtain

$$THDACPos_{1[DAC\ counts]} = \frac{\left[(maxBL_{2[counts]} + SixSigma_{[counts]}) * ADCstep_{[mV]} + Vshift_{[mV]} \right] - \left\{ (THDACBL_{2[counts]} * ADCstep_{[mV]}) + Vshift_{[mV]} \right\}}{THDACstep_{[mV]}} \quad (12)$$

After simplifying the terms of the equation we finally obtain

$$THDACPos_{1[DAC\ count]} = \frac{\left[(maxBL_{2[counts]} + SixSigma_{[counts]} - THDACBL_{2[counts]}) * ADCstep_{[mV]} \right]}{THDACstep_{[mV]}} \quad (13)$$

As can be seen in equation 13, the offset of the signal is cancelled. This means that the baseline and the peak value of the signal will be shifted by the same amount, and since the real energy value is reference to the baseline and not to ground, the effect of the offset is zero. Then the calibration can be focus only in the real gain of each channel.

14 Calibration

Calibration is an important part of the characterization of any electronic device intended to measure physical variables, and in the case of strip sensors it is not an exception. The calibration permits to achieve more precise results and hence a better data analysis of the readout information.

As it was mentioned in previous sections, there can be visible differences in the performance of the ASICs and since they are connected to a single strip sensor those differences are even more evident. The result is a system that behaves slightly different according to the position on the sensor that is covered by each ASIC. Even though this is a normal situation in multi-chip configurations, in order to have a reliable device it is necessary to minimize those differences and make it behave almost as a single chip device.

The way to accomplish a uniform behaviour of the system implies a deep understanding of the individual characteristics of each channel, and that is done comparing the performance of every channel when interacting with the same amount of charge/energy. Additionally, a single energy point is not enough, mainly because the performance of the system along the whole energy range is not always linear. In that case, in order to obtain good calibration results, several energy points along the ASIC's energy range are needed.

Ideally one would like to have several energy points well distributed along the chosen energy range of the ASIC, however in the case of higher energies, it would require an accelerator with tunable energy of the particles. Typically protons or alpha particles are used instead of photons which have low detection efficiency in silicon. The drawback of this method is that it requires measuring in vacuum in order to get precise results. Since the device was designed to work at room temperature, sensor and ASICs can reach higher temperatures, which means more noise added to the system. Additionally, the calibration parameters would need to be calculated for measuring at such temperatures. Instead one can use other techniques which require smaller and less complicated tools, and use resources easily available or even in the ASIC itself. These techniques can provide good enough results for most of the applications and analysis.

The architecture used in the ASIC to amplify and measure the energy produced by the ionizing radiation during the interaction with the sensor, theoretically provides a linear behaviour; however in reality it is usually not that linear in the whole energy range. Additionally, non-linearities can be added by the signal conditioning circuit. In this case, the calibration must include all the possible effects of the stages that the analog signal undergoes.

The energy of each channel is measured as an amount equivalent to the peak amplitude of the channels' output after being shaped and amplified by the readout electronics. All the channels having a valid event save the peak amplitude value in an analog memory; then the channels' information is available at the PD analog pin for reading out in sparsified mode and for later external digitalization. Here it is important to highlight once again that each voltage available at the analog pin is composed by the real amplitude of the event plus the baseline of the corresponding channel, as was shown previously in figure 39.

As it was described earlier, even though all the channels of an ASIC are fabricated on the same die, there are always small differences. These differences not only include the baseline level, but also an important part of the front end electronics: The amplification stage; Having

channels with slightly different amplification factors means that each channel has a different output voltage when measuring the same amount of energy. The problem is even worse if we take into account that the system uses four ASICs for a single strip sensor, and the strips are not connected to consecutive channels of the same ASIC but in interlaced configuration by ASIC pairs, as shown in figure 77. These problems affect negatively the resolution of the system making the Full Width at Half Maximum (FWHM) bigger. To solve these situations, a calibration procedure is necessary.

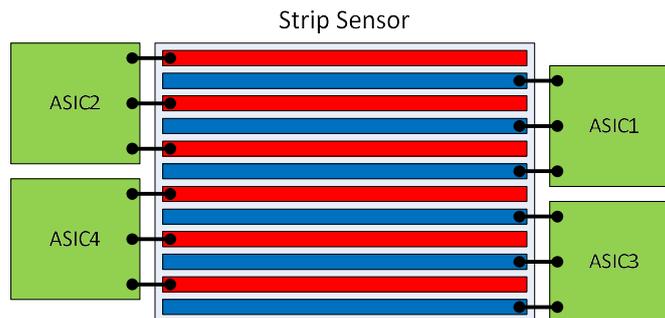


Figure 77. Interlaced connection of strip channels.

Additionally, the behaviour of the channels slightly changes when changing the amplification factor or the shaping time. The ASIC has three different amplification factors and four shaping times, giving as a result 12 different combinations. According to the target energy to be measured it is necessary to choose the combination that can offer better results and convenient measuring time, and then calibrate the system for that specific combination.

14.1 Calibration Methods

There are three basic ways to calibrate the ASIC's channels. The first one consists of applying external test pulses by a pulse generator. This method has the advantage of knowing the equivalent charge injected to the channels because it can be easily calculated. The main disadvantage is that this method doesn't include the whole detection loop (strip channel + readout electronics + analog to digital conversion circuit), and instead, the pulses are applied directly to the preamplifier of each channel, without taking into account possible effects coming from the strip sensor and PCB traces.

The second method is more comfortable because it uses the internal pulse generator of the ASIC to produce the input charge. Similarly to the first method, the charge injected to the system is well known, but it has the same drawback of the first method: it doesn't include the full loop that is used during real measurements. Additionally, a precise characterization of the test pulse generator is needed for each ASIC (linearity, real amplitude of the output signal, etc).

The last method is more precise (typically used), and includes the whole detection loop; Charged particles with well-defined energy (ideally mono-energetic) are used. The inconvenient of this method, as stated before, is the availability of radioactive sources or X-ray fluorescence XRF that can produce several energy peaks distributed along the whole energy range of the ASIC. Additionally, it is well known in XRF that the energy of the photons is always lower than the energy of the X-rays, which makes photons feasible mainly for lower energies.

In this thesis, the last two methods were used and will be explained in more detail next:

14.1.1 Calibration Using Internal Test Capacitors

This is the easiest way to debug or calibrate the system. Using the internal test capacitor available in each channel of the ASIC it is possible to inject charge to the preamplifiers as the interaction of a charged particle with the sensor would do. The amplitude of the pulse applied to the input of the channels is controlled by a single DAC; this basically provides the system with the possibility to cover the whole energy range, which is the main advantage of this method. The charge injected to each channel can be calculated as

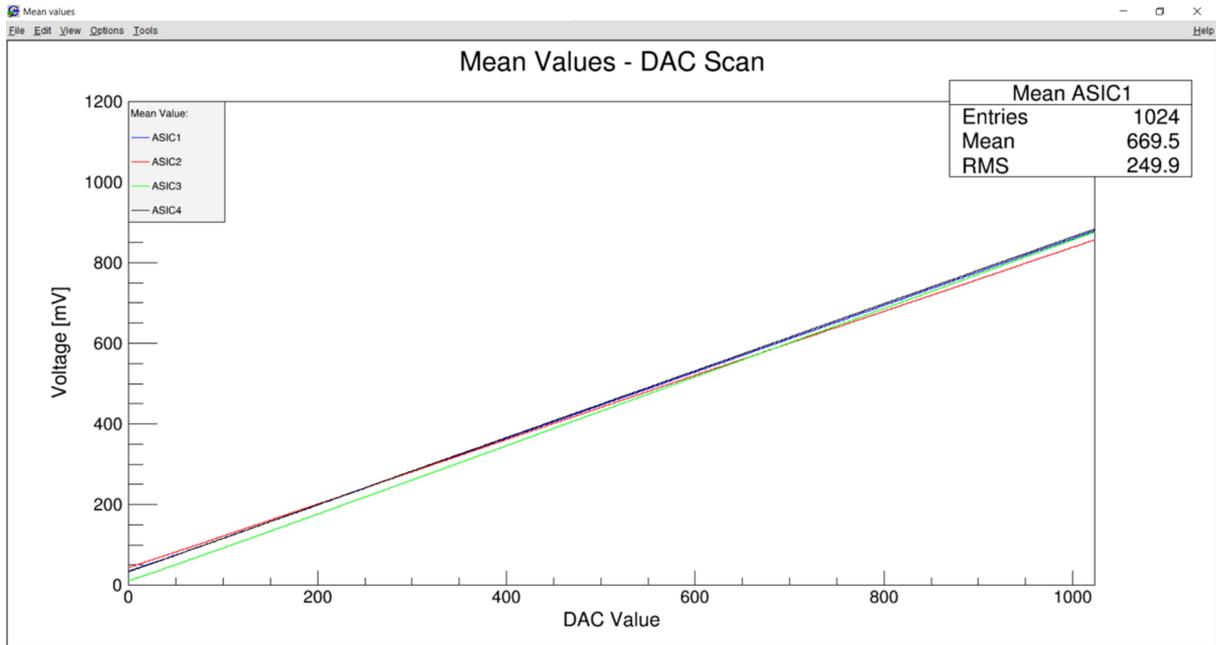
$$Q_{in} = \left(\frac{DAC_{val} * DAC_{step} + DAC}{5} \right) * C_{test} \quad (14)$$

where C_{test} is the capacitance of the channel's internal test capacitor (200fF). Applying hundreds or even thousands of pulses to each channel, a Gaussian distribution of the output values can be obtained. The mean value of the distribution along with the value calculated using equation 14, help in the estimation of the real amplification of each channel for a specific energy point, as shown in equation 15.

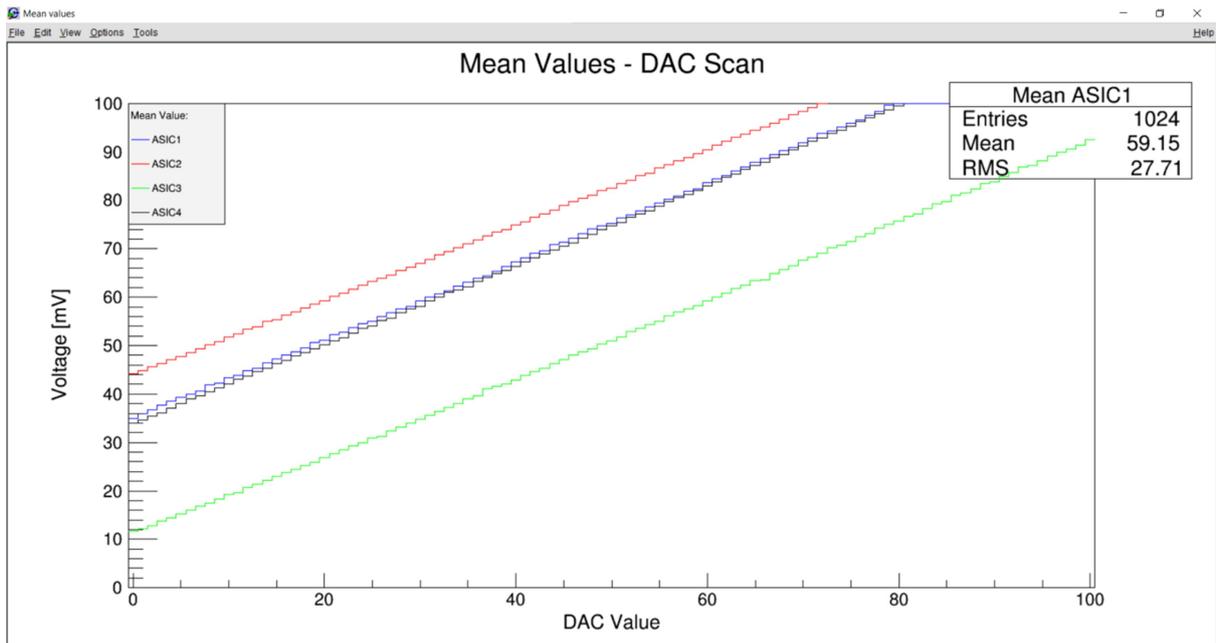
$$G_{Ch} = \frac{V_{o_{mean}}[mV]}{Q_{in}[fC]} \quad (15)$$

The real amplification factor of all the channels are considered as the calibration parameters of the system. If the system is linear, the gain of every channel is a constant value along the whole energy range, elseways curves must be used to model their behaviour. The calibration parameters are a key part in the calculation of the energy, and small deviations in the channel gain affect notably the produced energy spectrum.

This calibration method is very practical because everything can be implemented and measured within the system (without the need of external devices), however there is a second drawback in this method: the precision of the calibration depends on the reliability of the internal test pulse generator. As it was discussed before, the amplitude of the test pulse is set by a dedicated DAC, nonetheless this is not the only part involved in the pulse generation. There can be more effects produced by the pulse generator itself. In order to verify this situation, a scan of the test pulse generator was performed, and the results are shown in figure 78.



(a)



(b)

Figure 78. Test DAC scan: (a) full range, (b) baseline detail.

According to figure 78, when comparing the test DACs of 4 ASICs which belong to the same device, the overall performance of the test pulse generators looks pretty linear, but there are clear differences in their slope. Additionally, the baselines of the test DACs are not always similar and their values can be different from the theoretical one. This means that in reality all these differences make every ASIC's test pulse generator unique. In that case, a complete characterization of the pulse generation circuit of each ASIC is a must.

Furthermore, since long exposure times of the front-end electronics to radiation can progressively change the performance of the chip due to single event effects SEE [18], it is needed to re-characterize the test pulse generator of each ASIC after long measurement periods, just before starting this type of calibration; this increases the complexity and time of the calibration procedure.

Figure 79 shows the result of calibrating a device without taking into account the apparently small differences in the test pulse generators of the four ASIC.

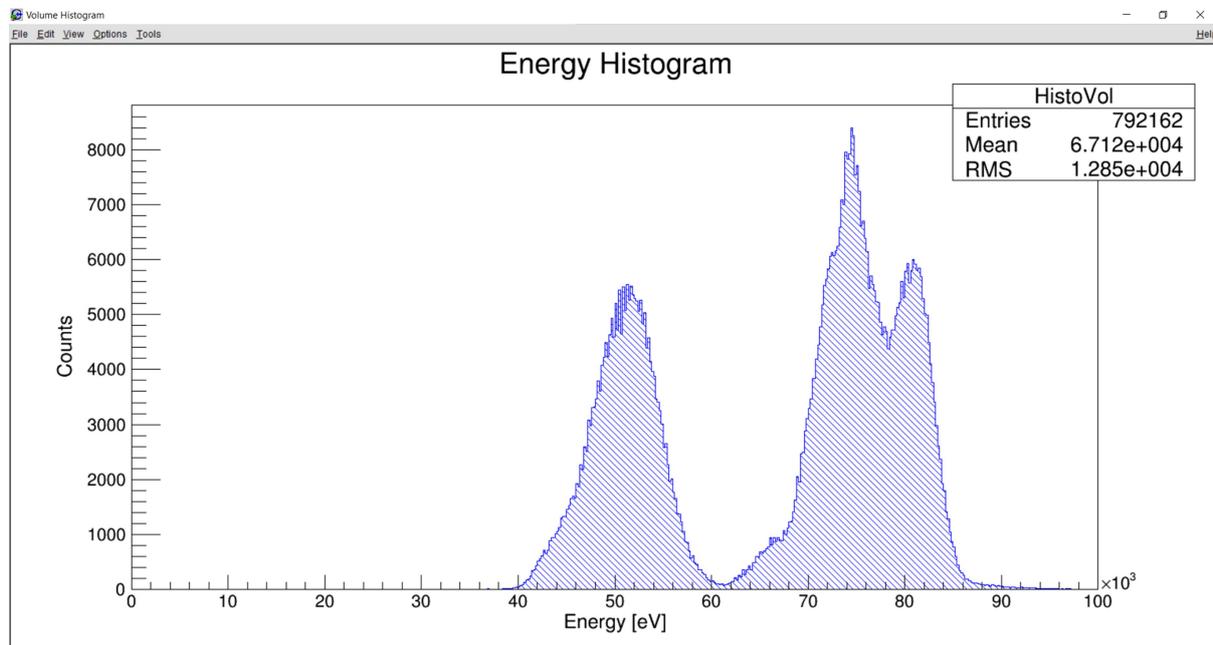


Figure 79. Incorrect energy spectrum of Zirconium XRF (15.74 keV) using calibration parameters based on test pulses, and without taking into account real parameters of the test pulse generators.

It is clear that without knowing the real slope and baseline of each test pulse generator, the calibration procedure is not really useful. The peaks shown in figure 79 are not only far from the real energy value, but also there should be a single energy peak. As the goal of this thesis is not a deep characterization of the ASIC's test pulse generator, the work was focused mainly in the calibration using ionizing radiation, which is a more common and precise calibration method.

14.1.2 Calibration Using Ionizing Radiation

This is a more precise way to calibrate the system compared to the other methods. Only drawback is the need of using radioactive sources. Usually it is recommended to measure at least three different energy peaks in order to have a good approximation to the behaviour of the channels, but it is clear that the more peaks used the more precise the calibration will be.

Figure 80 shows the setup used for the measuring of XRF (photons). During the measurements the whole system was shielded, not only by walls of lead bricks visible in the picture, but also by several lead layers on the top, as shown in figure 81. This is especially important to avoid human exposure to the radiation during data collection, especially in the case of photons due to their high capabilities of traveling in the air and production of secondary particles in surrounding materials.



Figure 80. Setup used in the measuring of XRF. A mini X-ray tube (AmpTek) was utilized to obtain XRF below 30 keV.

In figure 80 it can be seen that the strip sensor-based device was covered by a lead layer having a rectangular-shaped opening just in front of the strip sensor. This was done in order to protect the ASICs and other important components, as the FPGA and memories, from the radiation. The ASICs used in this thesis don't implement SEU(single-event upset)-tolerant circuits, which may lead to triggering of the channels by false acquisition logic when the activity of the source is too high. This is the case of the gamma photon source, which activity is 1.7 GBq. The situation previously described was not a problem when measuring XRF, however, the high flux of gamma photons produced several false events when no lead cover was used, as shown in figure 82. In any case, the false events are usually easy to identify during the data analysis due to their unusual values.



Figure 81. Complete shielding used during the measurements of XRF and gamma photons.

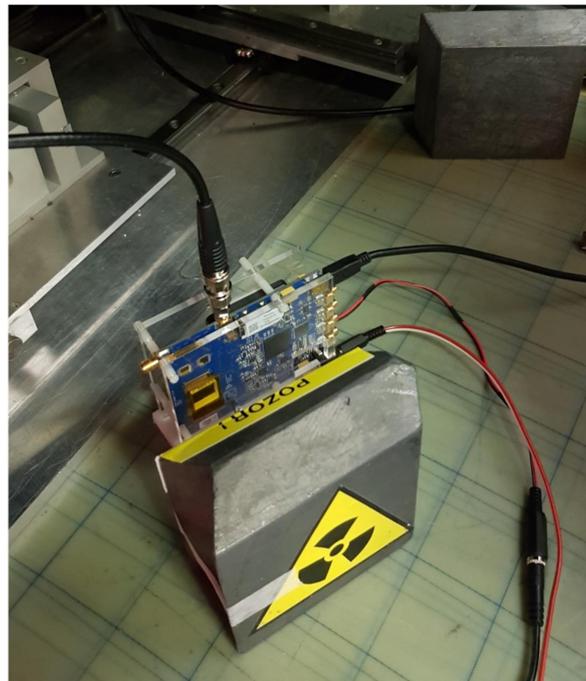


Figure 82. Measuring of gamma photons from ^{241}Am (1.7 GBq) without lead shielding on the device.

Coming back to the calibration process, as previously stated, there are three energy ranges selectable by choosing its corresponding gain. Since this type of calibration depends on the availability of radioactive sources, the calibration was performed for two of the three energy ranges in combination with one of the shaping times.

The first calibrated range covers low energy (<788 keV per channel) and has the best resolution of all the ranges. It is chosen by selecting the gain 57mV/fC. In order to calibrate this range, photons are the best option: they can travel freely in air without energy attenuation; however, there is a well known problem when detecting photons with silicon (material of the sensor): its efficiency is low, which means that the probability of an interaction of the photon within the sensor is low. To counteract this situation, longer measuring times are needed in order to collect enough statistics in every channel of the system. In any case, photons are a very useful mono energetic source for calibration of semiconductor detectors.

The second calibrated range is considered coarse compared to the lower energy range, but has the advantage of covering the maximum energy spectrum of the ASIC (up to 3.2MeV per channel). It is chosen by selecting the lowest gain (14.25mV/fC). This range is not the best option for measuring low energy particles since the resolution can make it difficult to distinguish peaks which are very close each other, or not far from the noise edge. This range is the best option to measure high energy particles, for example attenuated alphas, triton, etc., because the saturation level is much higher. For the calibration of this range alpha particles were used, however, since the alpha particles are attenuated in air, ideally one should measure them in vacuum. Unfortunately, the ASIC's maximum energy (3.2MeV) is lower than the standard energy of alpha particles (>5MeV). In that case, a Mylar foil could be used to reduce their energy, but at the expense of producing a much broader energy distribution of the alpha peak. Since the idea of the calibration is to use sources of radiation with thin energy peaks, measuring alphas in vacuum using a Mylar foil or measuring them in air gives similar results: the calibration will not be as precise as in the case of the calibration with photons.

The advantage of measuring alphas in air is not only that it is more comfortable but also that the temperature of the device (mainly the strip sensor and ASICs) can be easily kept at room temperature using the in-system incorporated fan. In that case, the option of calibrating this range in vacuum was not taken into account.

The third range is a middle point in resolution and range compared to the previous two cases. The drawback of this range is the difficulty to find calibration sources that can be measured by a thin silicon sensor and at the same time covering the upper part of the energy range. Taking into account that the range previously described covers all the energies up to 3.2MeV, the calibration of this range was not performed.

Regarding the lower energy range, two different sources of photons were used; photons produced by X-ray fluorescence XRF and photons produced by a gamma source. The X-ray fluorescence photons were obtained from Zirconium (15.74 keV), Molybdenum (17.44 keV) and Indium (24.14 keV), while the gamma radiation was obtained from Americium-241 (59.54 keV), and Cobalt-57(122.06 keV).

The calibration procedure starts by measuring each of the five energy peaks in each channel of the four ASICs. After cumulating enough statistics in each channel, each peak produces a distribution of events that can be modelled as a Gaussian function, as shown in figure 83.

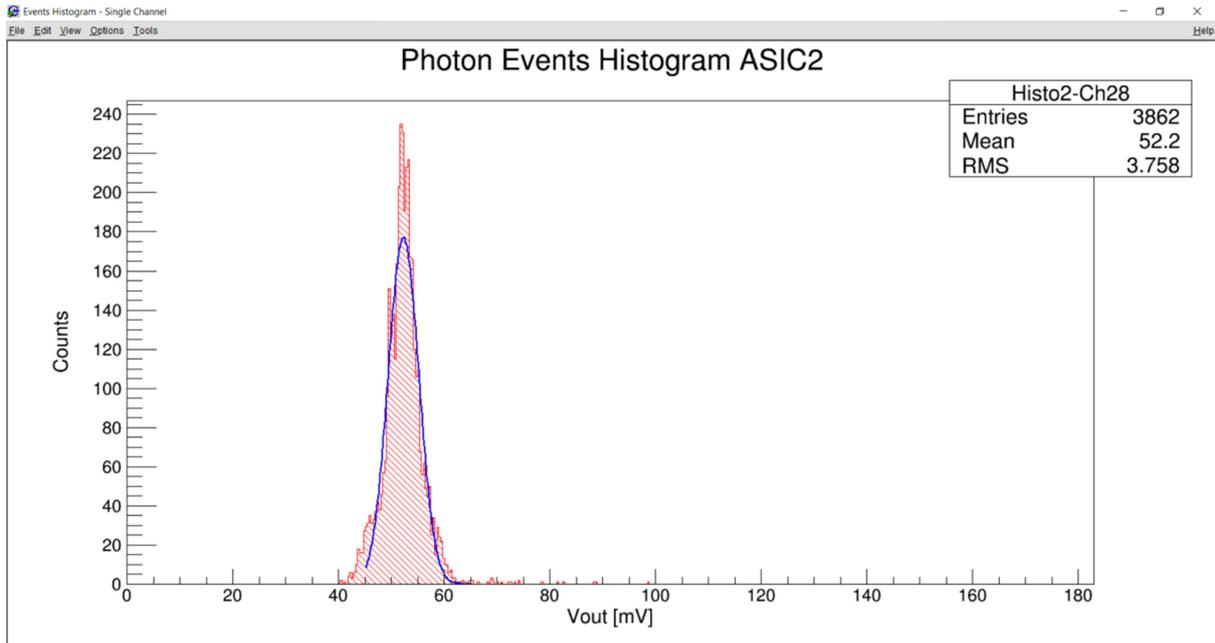


Figure 83. Events distribution of X-ray fluorescence from Molibdenum (red) and fitting Gauss function (blue) in channel 28, ASIC 2.

The mean value of the Gaussian distribution corresponds to the real amplitude of the signal for the channel. After calculating the mean value for all the channels and for the five energy peaks, a graph for each channel can be plotted, as shown in figure 84. Then a fitting function that matches the points must be found.

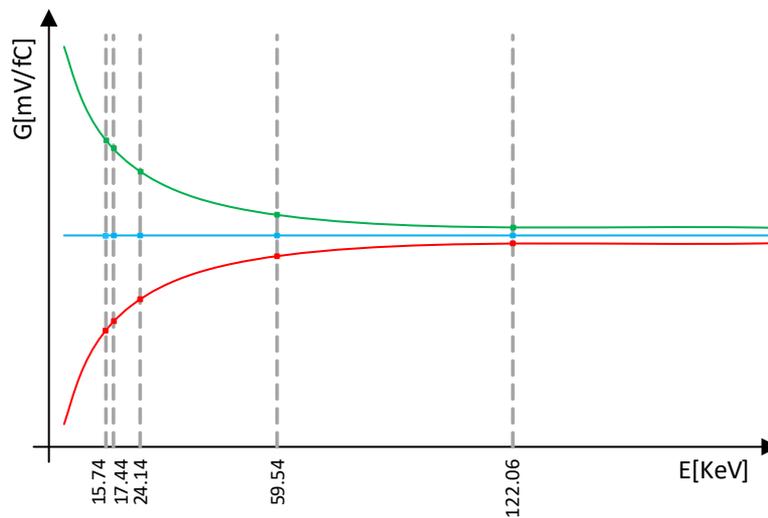


Figure 84. Gain vs Energy graph for three observed point distributions (green, blue, red). Five energy points were used in the calibration: Zr (15.74 keV), Mo (17.44 keV), In (24.14 keV), ²⁴¹Am (59.54 keV), ⁵⁷Co (122.06 keV).

As can be seen in figure 84, the distribution of the energy points is likely to be nonlinear, which makes the calculation of the gain more difficult. A simple and accurate function that matches the tendency is

$$G = a + \frac{b}{c+E} \quad (16)$$

where the parameters a , b and c are to be calculated by the fitting algorithm. The result of the fitting of all the channels is shown in figure 85.

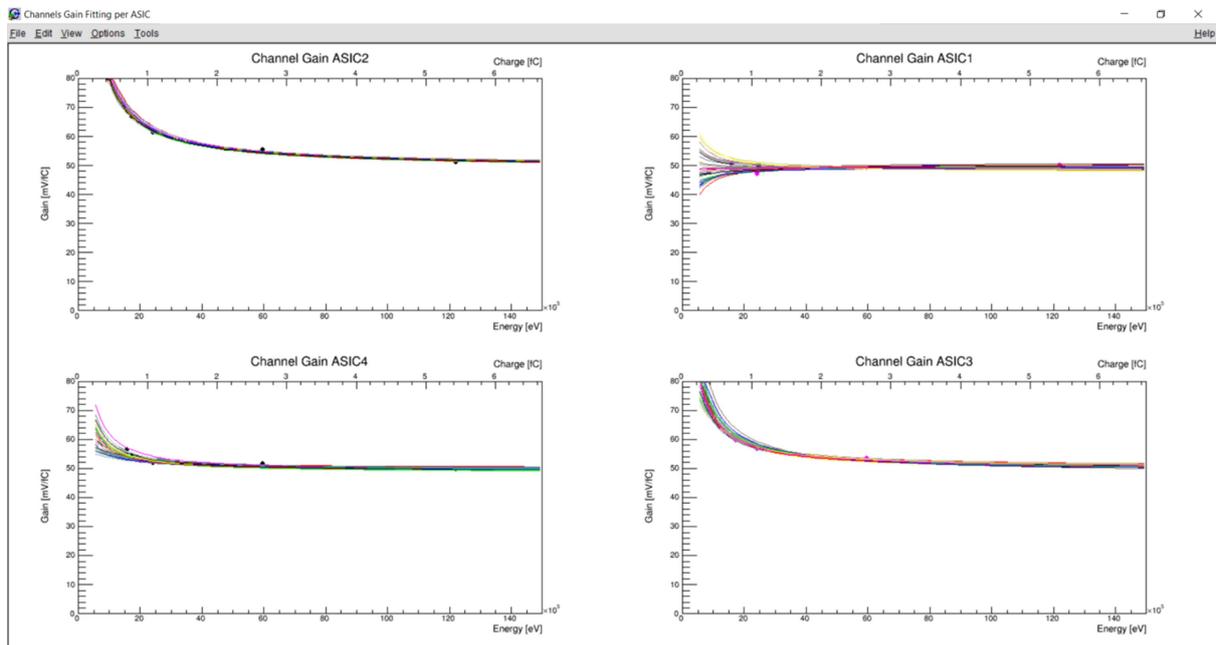


Figure 85. Fitting result for all channels in all four ASICs when calibrating the device using XRF and Gamma photons for Gain=57mV/fC, shaping time=500ns.

Since equation 16 relates gain and energy, and the real gain of each channel along the whole energy range is unknown, the energy calculation is not straightforward. To solve that situation an additional equation must be used. This equation is

$$E = VO_{[count]} * \frac{adcstep * ionSi}{G * e^{-} * 10^{15}} \quad (17)$$

Equation 17 calculates the energy for a given output voltage when the gain of a channel is known. Using equations 16 and 17, a function which relates energy in terms of the output voltage can be obtained. The new equation is very useful since it helps calculating the energy

of an event directly from the output voltage of the channel independently from the actual gain value.

The energy for a given event in a channel can be calculated as

$$E = \frac{R - b - a * c + \sqrt{(a * c + b - R)^2 + 4 * a * c * R}}{2 * a} \quad (18)$$

where

$$R = \frac{Vo_{[count]} * adcstep * ionSi}{e^- * 10^{15}}$$

Parameters a , b and c are the calibration parameters, and along with the equation 18, one can fully describe the behaviour of each channel in the selected energy range.

Figure 86 shows the resulting energy spectrum for different energies when no calibration is used (a global theoretical gain of the ASIC is used), while figure 87 shows the result after applying the calibration parameters for each channel.

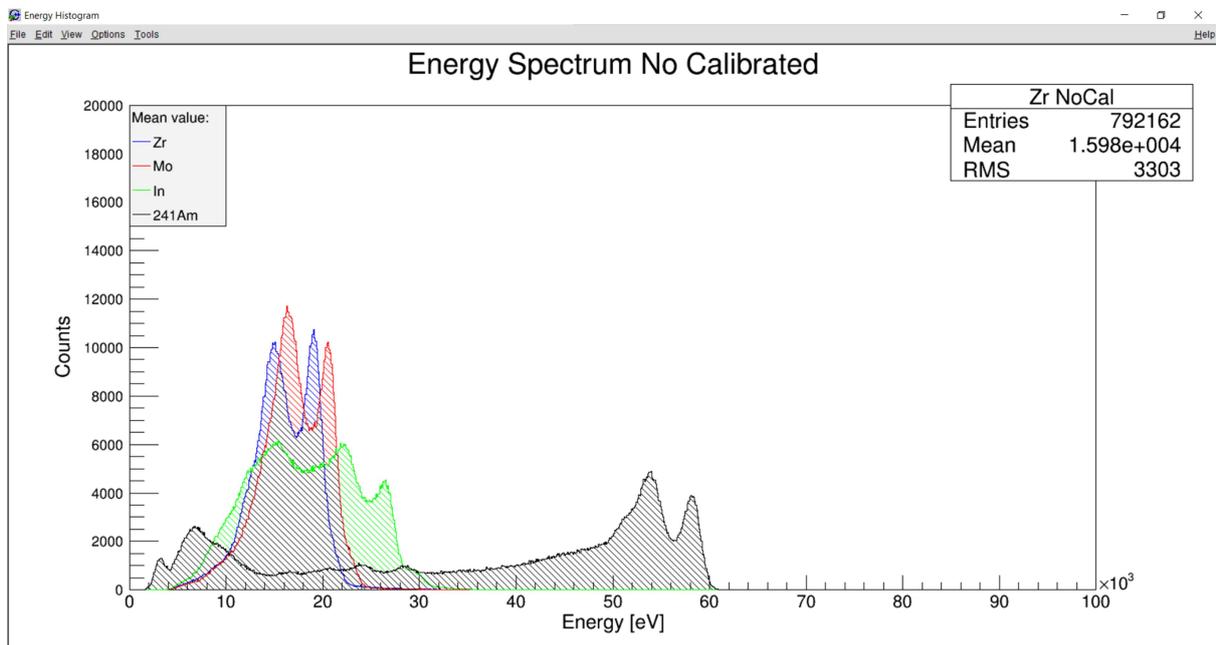


Figure 86. Superimposed energy spectrum of Zirconium, Molibdenum, Indium and 241-Americium photons using Gain=57mV/fC, shaping time=500ns without calibration.

In figure 87 it can be seen that the calibration parameters work correctly; the energy peaks are centered at the right position and there is a single peak for each energy line (opposed to what is shown in figure 86). In the case of the gamma photons from ^{241}Am , due to the high activity of the source, it is possible to see not only the more intense peak (59.54 keV) but also less intense peaks as 26.4 keV or 17.8 keV. When measuring XRF from Indium, a second peak appears at lower energies (left peak). This second peak is not caused by the system itself but instead it was produced by secondary particles. The reason why the measurement of the Indium peak was notably more affected by the Lead fluorescences is because of the small size of the indium target used. Since the X-ray beam is conic (120°) and not point-like, there were big chances for the photons to interact with the setup's surrounding lead shielding plus possibly other materials at the bottom of the setup. Furthermore, the sigma value of the system was calculated as 1.6 keV in the range 15 to 60 keV. For the same energy range, Timepix devices can provide a sigma value up to 2.3 keV [1].

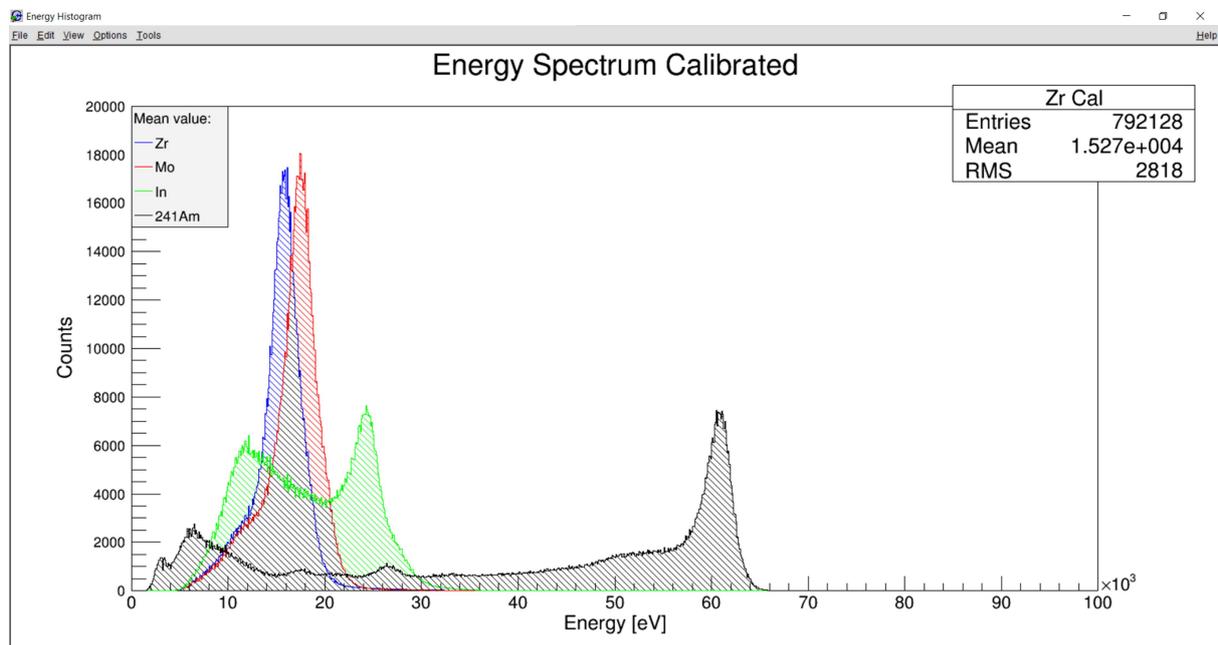


Figure 87. Superimposed energy spectrum of Zirconium, Molybdenum, Indium and 241-Americium photons using Gain=57mV/fC, shaping time=500ns without calibration.

Regarding the calibration of the higher range, as mentioned before, alpha particles from americium-241 were used. In order to obtain different energy peaks, the distance between the source and the surface of the strip sensor was changed, as shown in figure 88.

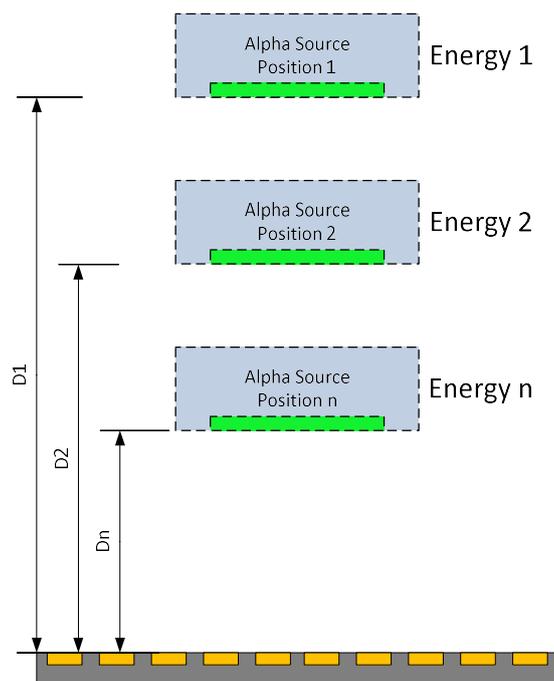


Figure 88. Method used to obtain alpha particles with different energy in air.

As in the case of the calibration with photons, five energy points were chosen: 0.5MeV, 1MeV, 1.5MeV, 2MeV and 2.6MeV. Then it was necessary to calculate the right source-sensor distance for each selected energy. This was done in a fast and precise way using available Range-Energy experimental curves for alpha particles in air. The procedure of the calculation is shown in figure 89.

Using figure 89, the source-sensor distance is calculated projecting the alpha's full energy (5.48MeV - red line) and the wanted energy of the alpha particle (blue line) on the graph's range axis. Then the distance corresponds to the difference between the two projected values. From the graph, the resulting distances were 37.2mm (0.5MeV), 35.1mm (1MeV), 32.8mm (1.5MeV), 30.2mm (2MeV), and 26.5mm (2.6MeV).

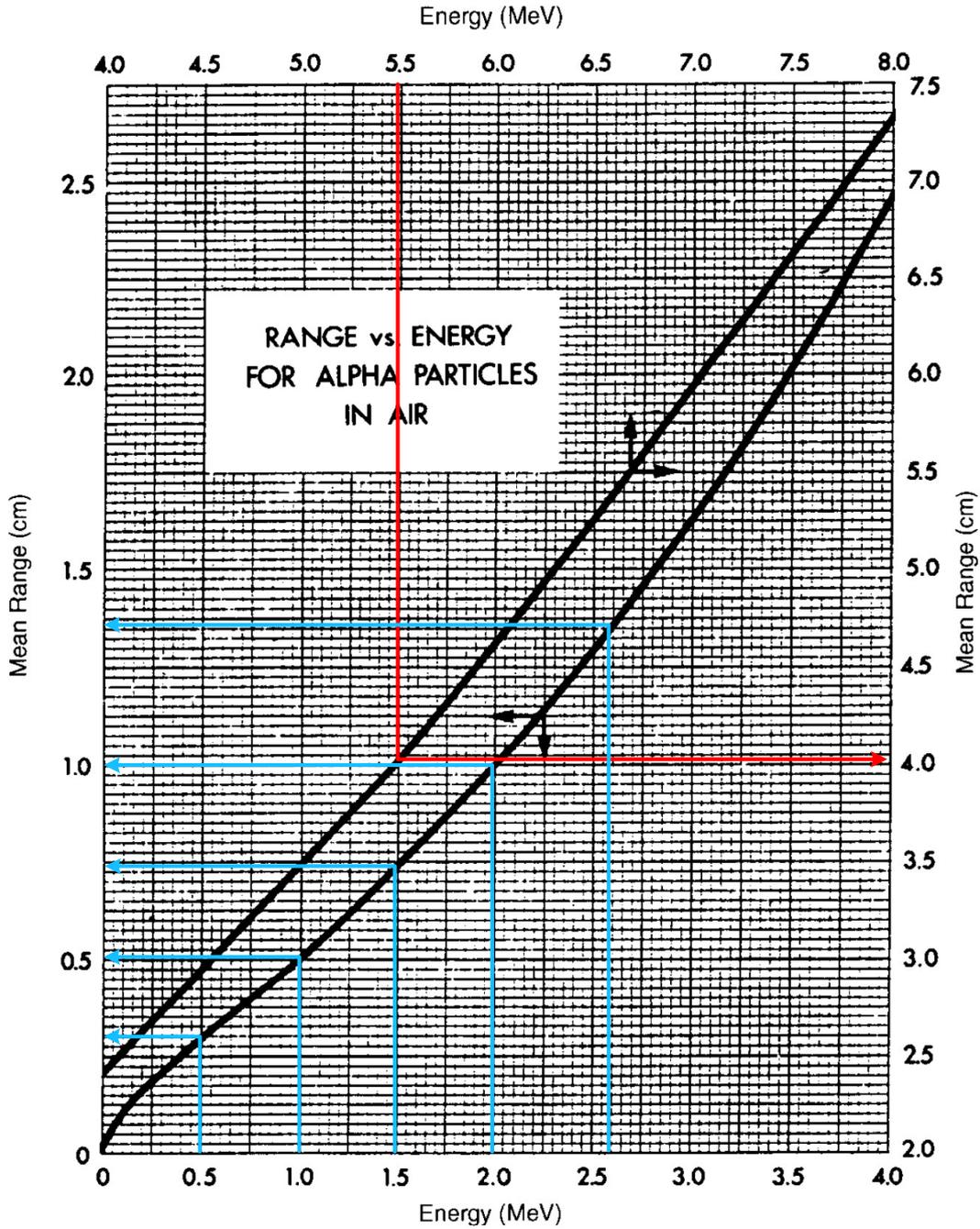


Figure 89. Calculation of source-sensor distance for alpha particles in air. Chart taken from [7].

Using alpha particles in air for calibration has a clear limitation, which is explained based on figure 90. Basically, the point in the source from which the alpha particle is produced and the interaction point on the strip sensor varies, meaning that the alpha particles travel different distances and hence they arrive with clearly different energy at the sensor. This makes this method only a demonstrative way of calibration, but it can not be considered a precise result as in the case of the calibration with photons. Additionally, the distances calculated here

correspond to the energy of the alpha particle when traveling vertically, meaning that any other trajectory generates lower energy events and hence broadening of the alpha peak.

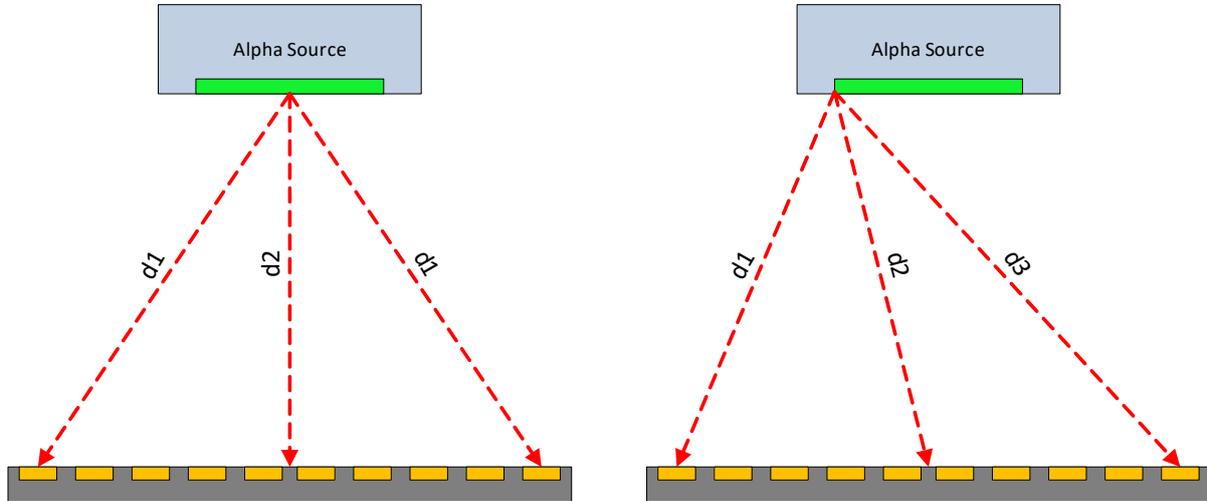


Figure 90. Example of some possible trajectories of the alpha particles in air when the decay was in the middle (left), and at one end of the source (right).

To obtain the calibration parameters, the same procedure and equations were used as for the previous range. Figure 91 shows the fitting curves for all the channels of the device.

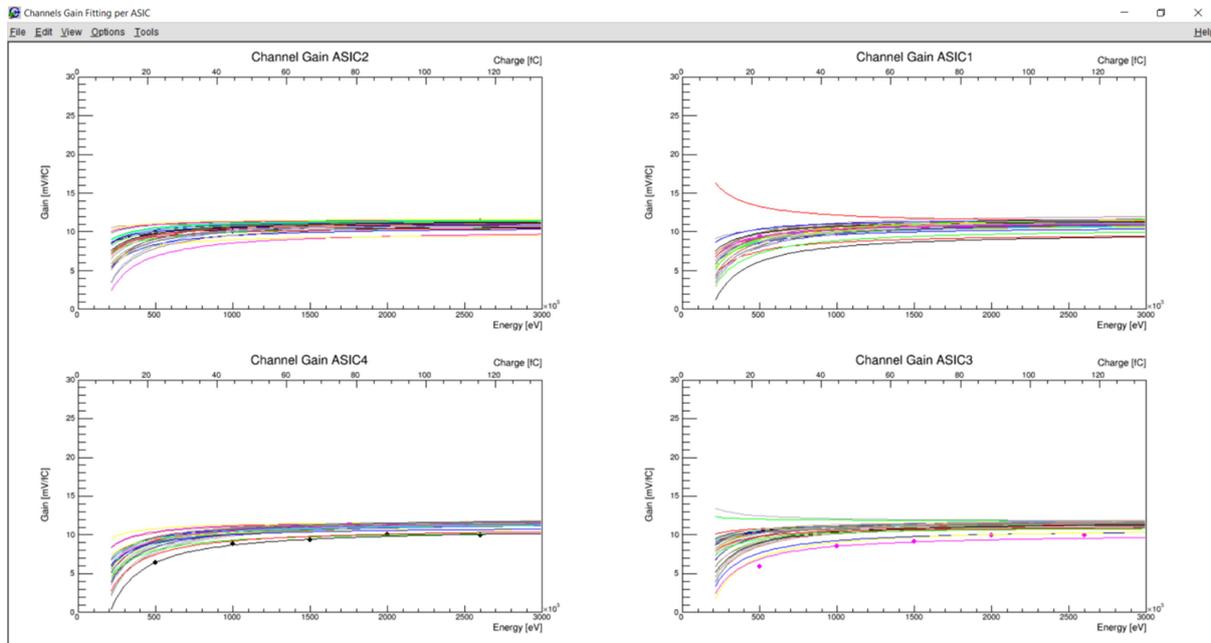


Figure 91. Fitting result for all channels in all four ASICs when calibrating Gain=14.25mV/fC, shaping time=500ns and using alpha particles from 241Am.

In order to verify the result of the calibration, a three energy peak alpha source was measured. The source contains alphas from Plutonium-239, Americium-241, and Curium-244. In this case, the source-sensor distance was fixed to 32.8 mm. This distance was chosen to provide energy values within the higher range of the ASIC without saturating the channels, and avoiding having events too close to the noise edge. Using figure 92 the energy calculated for each alpha peak (for vertical trajectory) was 0.72MeV (Pu), 1.52MeV (Am), and 2.22MeV (Cm).

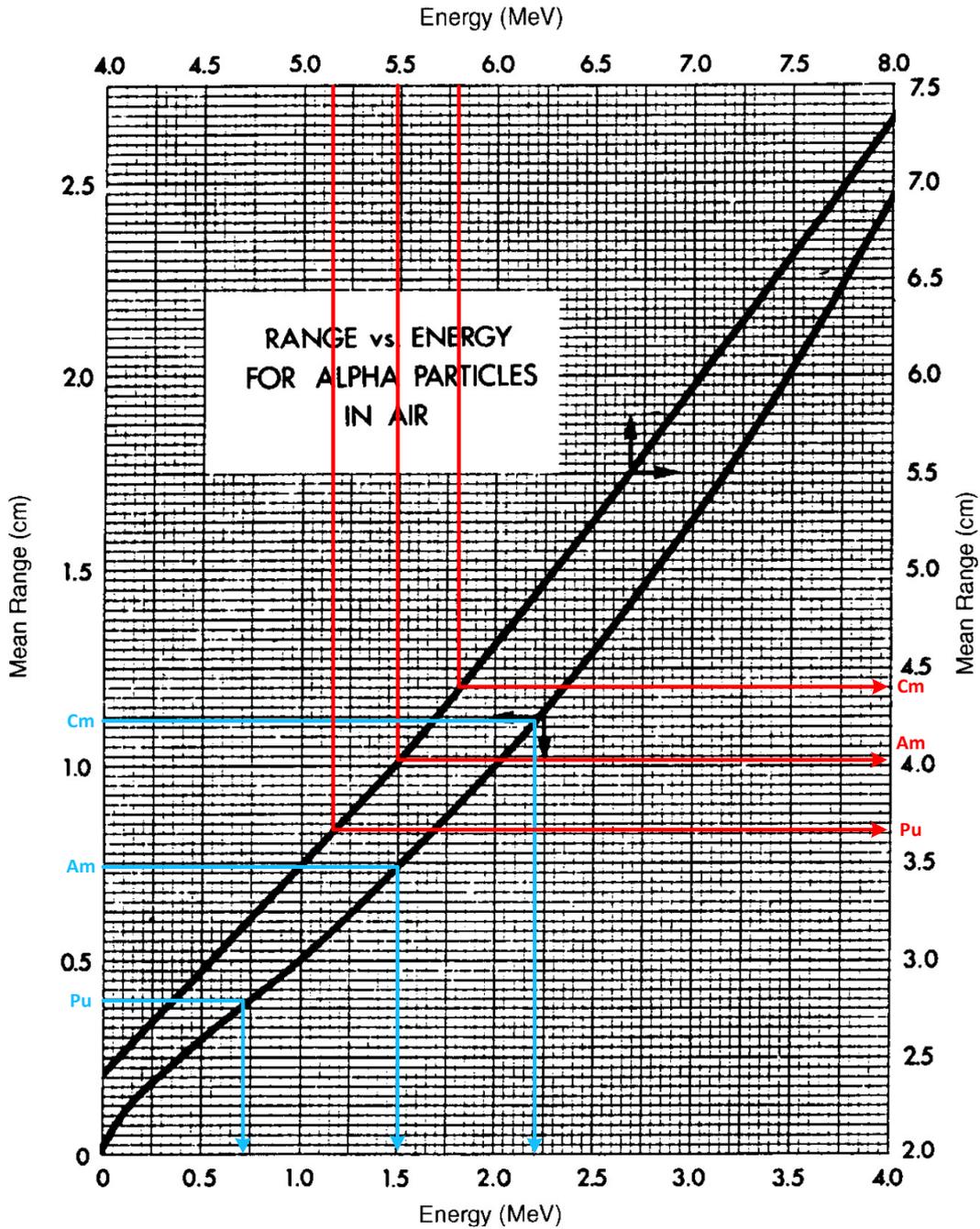


Figure 92. Calculation of PuAmCm alpha particles's energy in air (distance=32.8mm). Chart taken from [7].

Figure 93 shows the data measured when no calibration parameters were used (using default global gain), while figure 94 shows the result after using the approximate calibration parameters.

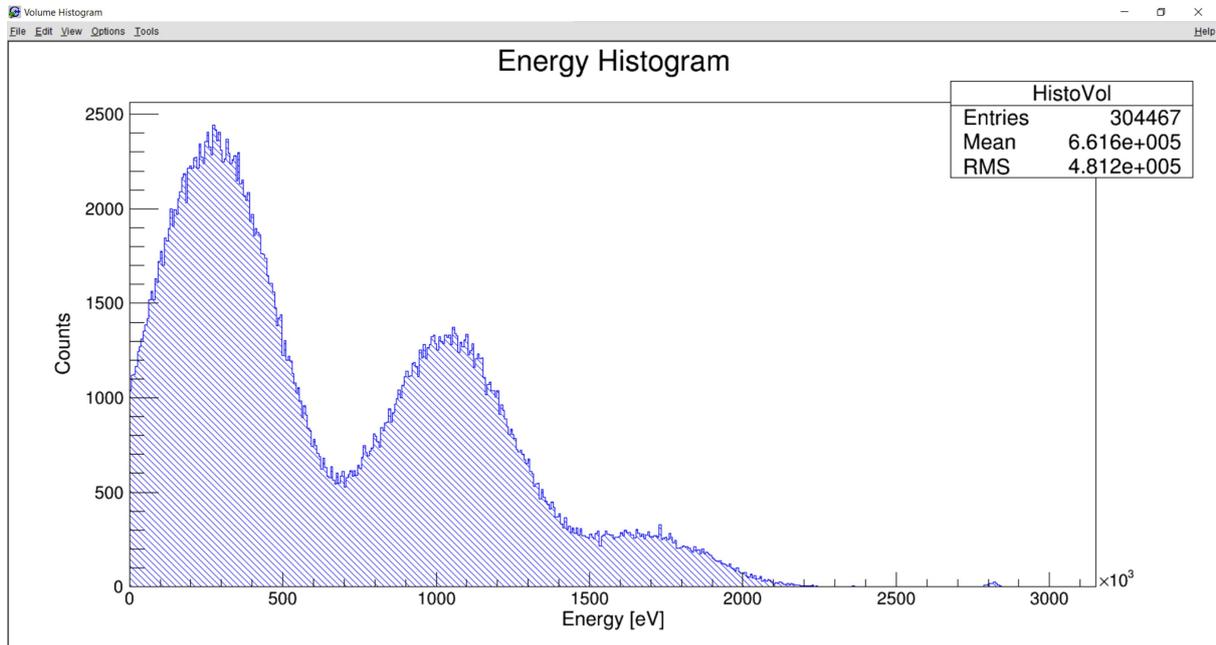


Figure 93. Energy spectrum of PuAmCm alpha particles in air for a distance of 32.8mm (without calibration).

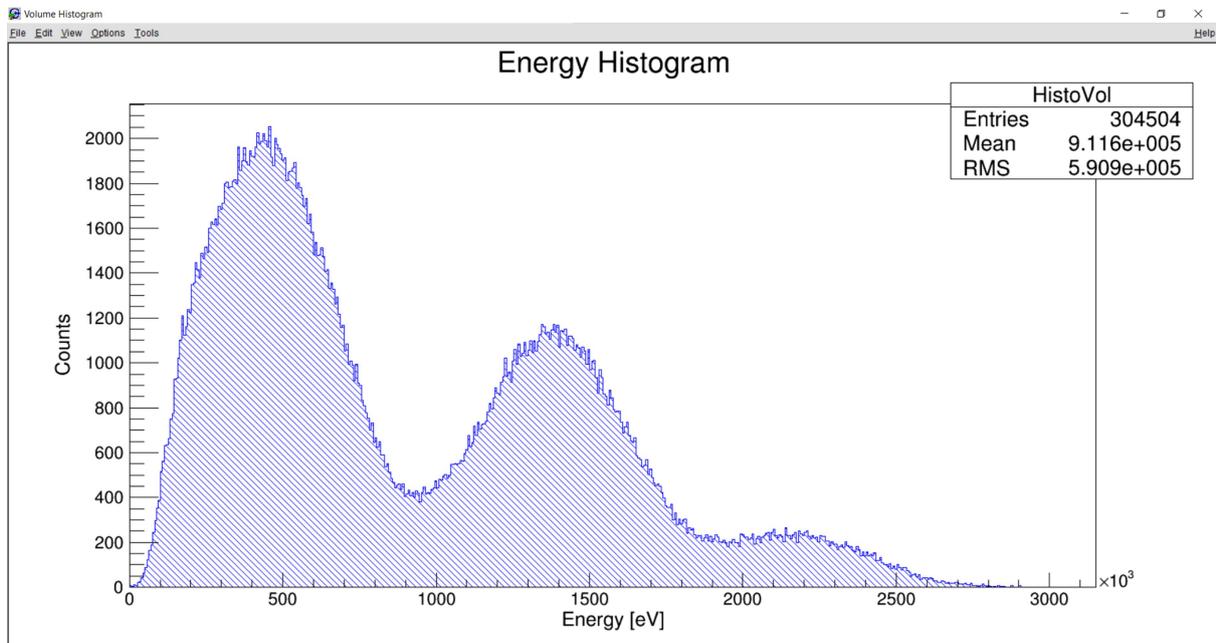


Figure 94. Energy spectrum of PuAmCm alpha particles in air for a distance of 32.8mm after calibration.

It is clearly visible in figure 93 the result of using alpha particles in air as a calibration source; as stated before, alpha particles in air produce a range of energy instead of a single energy peak due to different trajectories. For a correct calibration is always needed a mono-energetic source of radiation.

Even though the calibration parameters were calculated based on inaccurate energy values, figure 94 shows that the mean value of each peak was moved towards the right energy values, having the higher energy peak centered at the right position. This shows that even having these inaccuracies in energy of the alpha particles, the calibration method works quite fine.

15 Conclusions

The research carried out in the presented thesis was focused on exploring the capabilities of strip detectors as an alternative mean of radiation detection and measurement. Several important advantages of strip detectors compared to the broadly used hybrid detectors (pixel detectors) were evinced: the inherent separation of the readout electronics (ASICs) and the sensor makes possible for the incoming particles to go through the sensor without interacting with the readout ASICs, consequently reducing the probability of single event effects and prolonging the front-end electronic's lifecycle. Additionally, the ASICs can be easily shielded without affecting the particles' path. Another advantage of the ASICs-sensor separation is that the heat produced by the readout electronics is not transferred to the sensor, avoiding changing the sensor's performance due to varying temperature; furthermore the ASICs can be cool down independently from the sensor. One more advantage is the price; strip detectors are much cheaper than pixel detectors as long as the ASIC's size and design are not limited by the pixel size. Besides, the micrometric and complex bump-bonding process is not needed, and they can be fabricated in big sizes, different pitches and shapes. This is especially important in applications where big areas are to be covered. Finally, damaged ASICs or sensor can be easily exchanged, which is not possible in the case of pixel detectors.

The 128-channel strip sensor-based system was successfully used as spectroscope, measuring alpha particles, XRF and gamma photons at room temperature. Since the system is composed of 4 ASICs connected to a single strip sensor, the differences ASIC to ASIC or channel to channel are more evident, which means broader energy spectrum or even multiple peaks for a single energy. In order to get a uniform performance of the system, custom equalization and calibration procedures were developed, analysing the characteristics of every channel independently. These procedures showed a remarkable enhancement of the energy spectrum, which is a typical problem in multichip configurations. The system provides a sigma of 1.6 keV when measuring XRF and gamma photons in the energy range 15-60 keV, taking into account all the 128 channels. This result is promising if compared to Si hybrid-pixel detectors typically having a sigma of 2.3 keV [1]. Furthermore, even having a conservative approach of 6-sigma distance to the electronic noise level, the threshold of the system was about 3 keV.

There are clearly two key components in the system: ASICs and strip sensor. The ASICs define the features and performance of the system while the sensor defines the type of particles that can be detected and detection efficiency depending on the energy of particles. However, there is an important component linking all the constituent parts of the system together: PCB. The importance of a good PCB design in a mixed-signal system was evinced during the development of the two system versions shown in this thesis. Extremely sensitive analog signals can be easily distorted by digital signals if the PCB design doesn't counteract cross talk and EMI correctly. The PCB was designed following recommendations for mixed-signal systems; however there is not a precise set of rules to guarantee the best result as long as every system has unique characteristics. The system works according to expectations, however the FWHM can be lowered by a redistribution of components on the PCB and by reducing the number of components involved in the signal conditioning circuit.

Although strip sensors have usually been used as counters or trackers, thanks to new generation of ASICs it is possible to use them as spectroscopes hence broadening the fields of application. Potential applications can be mentioned: single event effect detection, tracking,

dosimetry, and X-ray imaging, among others. In the case of an application requiring position detection, since a single strip sensor is able to provide only one dimension, a pair of strip detectors is needed in order to create a coordinate system. Additionally, the measurements will be restricted to highly penetrating particles due to the need of having events produced by a single particle in two independent sensors. When measuring heavy particles, a better solution for position detection is a double-sided strip sensor which can provide position and energy measurement within a single sensor. The only limitation of double-sided strip sensors is that phantom events can be created when the maximum particle rate of the system (calculable) is exceeded.

In addition to the work presented in this thesis, feedback was provided to the designers of the ASIC in BNL, especially to the head of microelectronics Dr. Gianluigi De Geronimo and to the mixed-signal IC designer Ing. Wenbin Hou. The feedback was based on the results of the characterization and tests made to the ASICs, and to the whole system including the strip sensor, mainly when working at their maximum speed. This provides them with interesting and useful information for the design of new ASIC generations.

Future work should be focused on using bigger, thicker and different materials of sensors in order to increase the efficiency of the system when measuring photons, betas or other type of particle requiring higher cross section materials to be detected. Even though the system shown here uses a relatively small strip sensor, the components, design of the system, equalization and calibration processes contain all the basic features for systems based on any size of strip sensor. Moreover, a new approach using double-sided strip sensors can be fabricated and study in more detail.

Bibliography

- [1] J. Jakubek, “Precise energy calibration of pixel detector working in time-over-threshold mode”, *Nuclear Instruments and Methods in Physics Research A* 633 (2011) S262–S266.
- [2] G. Aad, et al., “The ATLAS Inner Detector commissioning and calibration,” in *The European Journal of Physics C*, DOI 10.1140/epjc/s10052-010-1366-7, Springer, 2010.
- [3] ATLAS Collaboration, “Operation and performance of the ATLAS semiconductor tracker,” in *JINST*, 2014.
- [4] G. Lutz, *Semiconductor Radiation Detectors*, 2nd ed. Heidelberg, Germany: Springer, 2007.
- [5] H. Spieler, *Semiconductor Detector Systems*, 1st ed. NY, USA: Oxford University Press, 2005.
- [6] S. N. Ahmed, *Physics and Engineering of Radiation Detection*, 2nd ed. Oxford, UK: Elsevier, 2015.
- [7] G. F. Knoll, *Radiation Detection and Measurement*, 4th ed. NY, USA: John Wiley & Sons, Inc., 2010.
- [8] C. Grupen and B. Shwartz, *Particle Detectors*, 2nd ed. NY, USA: Cambridge University Press, 2014.
- [9] G. De Geronimo, et al., “Front-End ASIC for a Silicon Compton Telescope,” in *IEEE Transactions on Nuclear Science*, Vol. 55, No 4, August 2008.
- [10] S. Watanabe, et al., “Development of Semiconductor Imaging Detectors for a Si/CdTe Compton Camera,” in *Nuclear Instruments and Methods in Physics Research. Sec. A* 579, 2007, pp. 871–877.
- [11] E. Barberis, et al., “Capacitances in Silicon Microstrip Detectors,” in *Nuclear Instruments and Methods in Physics Research. Sec. A* 342, 1994, pp. 90-95.
- [12] V. Kulibaba, et al., “Interstrip Resistance of a Semiconductor Microstrip Detector,” in *Questions of atomic science and technics, Series: Physics of radiation effects on radio-electronic equipment. Sec. 39*, 2001, pp. 180-182.
- [13] AEGIS Collaboration, “AEGIS experiment commissioning at CERN,” in *AIP Conf. Proc.* 1521, 144, 2013.
- [14] A. Kok. (2015, Apr. 13). AEGIS – Sample strip sensors [online]. Available e-mail: Angela.Kok@sintef.no
- [15] G. De Geronimo and Paul O’Connor, “MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers,” in *IEEE Transactions on Nuclear Science*, Vol. 52, No 6, December 2005.
- [16] Brookhaven National Laboratory - Instrumentation Division, “NCIASIC3”, ASIC datasheet, Release 5/10/2012.

- [17] G. De Geronimo, et al., “A CMOS Baseline Holder (BLH) for Readout ASICS,” in IEEE Transactions on Nuclear Science, Vol. 47, No 3, June 2000.
- [18] C. Boatella. (2017, May 9). “Radiation Environment and its effects in IEEE components and hardness assurance for space applications,” in CERN - ESA - SSC Workshop [online].