130 nm CMOS Fully Differential SC Filter for Ultra-Low Voltage Σ-Δ Converter

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Abstract—In this paper design and function of the fully differential (FD) switched-capacitor (SC) integrator for ultra-low voltage Sigma-Delta analog to digital converter (Σ-Δ ADC) are presented. The proposed integrator was designed for differential input signal and applicable as a main analog block of ultra-low voltage Σ-Δ ADC in standard 130 nm CMOS technology. The main block of proposed integrator is operational transconductance amplifier (OTA) based on two-stage Rail-to-Rail (RtR) FD operational amplifier (OPAMP) working in sub-threshold regime. The characteristic properties of this circuit is non-standard OTA topology, using SC common-mode feedback (CMFB) circuit and using switching T-gates. All of these subcircuits are supplied by only 0.6 V with achieved gain 24.09 dB and cutoff frequency 165.95 kHz.

Keywords—analog design, ultra-low voltage, switched-capacitor integrator, Sigma-Delta ADC, CMOS

I. INTRODUCTION

Nowadays, analog designers are facing difficult challenges due to evolution of CMOS nanometer technology and continuous scaling-down of the power supply voltage of integrated circuits (IC). These things cause decreasing dimensions of transistors and affect to the properties of the analog circuits. Usage of transistors as resistors, capacitors, amplifiers or current sources is still needed in analog design but the requirement to minimize the supply voltage brings many problems. For example, more than 2 or 3 transistors cannot be stacked because of the voltage headroom issue. In addition, many of them work in weak inversion region where current $I_D$ exponentially depends on voltage $V_{GS}$ and where is considerable parasitic capacitance effect. On the contrary, in digital design, transistors are mostly used as the switches and there are not so many problems of this kind with them. It is one of the most important advantage of digital ICs.

ADCs has been moved to the CMOS nanometer technologies as an interface between analog and digital circuits. Both of these kinds of circuits are implemented on single chip, so they have to be power-supplied by one $V_{DD}$ voltage. Since the digital part of the circuit can operate with an ultra-low supply voltage, the analogue parts of the circuit are adapted to these ultra-low values of $V_{DD}$ as much as possible. In Σ − Δ ADC is low-pass filter - integrator the main block of the analog part of the circuit. It causes the pulses to densify on the digital output signal, Compared to the input, the shape of the signal is different, but its nature is preserved [1], [2], [3].

Fig. 1 shows differential block scheme of Σ − Δ ADC. In this scheme, analog input signal is compared (by difference amplifiers) with reference signal coming from 1 - bit digital to analog converters (DACs). This modified signal is then integrated and compared to the reference voltage in comparators (in generally 0 V). Then looped to 1-bit DACs whose outputs are changing mentioned analog input reference in the difference amplifiers. D-type flip-flops are used for synchronization of digital output signal [4].

II. PROPOSED INTEGRATOR

Topology of FD SC integrator block from Fig. 1 is introduced in the Fig. 2.
A. Operational transconductance amplifier - OTA

The topology of OTA is shown in the Fig. 3. This circuit is based on parallel connection of two-stage NMOS and PMOS OPAMPs working in sub-threshold regimes.

![Fig. 3. Topology of OTA](image)

Complementary connection of NMOS and PMOS in the OPAMP output stage allows RiR operation at output. It is well-know that input voltage range of PMOS transistor is limited from above by the voltage:

\[ V_{PMOS_{MAX}} = V_{DD} - |VDS_{sat}(i_{MP7})| - |VT_{H}(i_{MP1})| \]  

(1)

In the range from \( V_{PMOS_{MAX}} \) to \( V_{DD} \) is NMOS transistor active only. Contrariwise, the input voltage range of NMOS transistor is limited from below by the voltage:

\[ V_{NMOS_{MIN}} = V_{DS_{sat}(i_{MN8})} + VT_{H}(i_{MN1}) \]  

(2)

In the range from ground to \( V_{NMOS_{MIN}} \) is PMOS transistor active only.

Around the \( \frac{V_{DD}}{2} \) voltage, both of transistors are in the active region. In the area where both amplifiers operate in the active region, the transconductances \( g_m_{NMOS} \) and \( g_m_{PMOS} \) are overlapped. In general, by increasing \( g_m \), the dominant pole is shifted towards higher frequencies. This may result in frequency response and overall circuit stability. Transistors \( i_{MN1}, i_{MN2}, i_{MP1} \) and \( i_{MP2} \) have been designed with \( g_m \) compensation as is shown in Fig. 4:

![Fig. 4. Compensation of \( g_m_{PMOS} \) and \( g_m_{NMOS} \)](image)

The input transistors \( (i_{MN1}, i_{MN2}, i_{MP1}, i_{MP2}) \) was set to the sub-threshold region by the equations:

\[ V_{eff} = 2V_{T}.n\ln(exp(\sqrt{TF}) - 1) \]  

(3)

\[ \frac{W}{L} = \frac{I_D}{I_{D0}exp\left(\frac{V_{DD}}{nV_{T}}\right)} \].  

(4)

The current sources \( (i_{MP7}, i_{MN8}) \) works in strong saturation by the \( V_{DS} \) voltage approximately 100 mV. Transistors \( i_{MN7}, i_{MN9} \) and \( i_{MP8} \) was used as the simple current mirrors for circuit biasing. \( i_{MP4}, i_{MP5}, i_{MN4} \) and \( i_{MN5} \) was used as a current mirrors for output stage 1 and 2 [5].

As an output stage, AB class amplifier is used. Dimensions of the transistors \( i_{MP3}, i_{MN3}, i_{MP6} \) and \( i_{MN6} \) was designed for relatively high currents in that branches due to driving output capacitors and capacitors in CMFB circuit.

B. Clock-boost circuit

In order to control switching transistors in CMFB circuit clock-boost circuit was used. Its topology is shown in the Fig. 5. Two inverters at the beginning of the circuit modify the rising and the falling edges of the clock signal for better operate with. Cross-coupled NMOS transistors \( b_{MN1} \) and \( b_{MN2} \) together with the capacitors \( b_{C1} \) and \( b_{C2} \) are forming a charge pump. Pulses from the clock are shifted up by adding \( V_{DD} \) voltage to them. By the transistors \( b_{MN3} \) and \( b_{MN4} \) is this shifted voltage (in the other words: shifted charge) connected to a "bootstrap" capacitor \( b_{C3} \). By switching the transistors \( b_{MP1}, b_{MN5}, b_{MP2}, b_{MN6}, b_{MN7}, b_{MN8} \) and \( b_{MN9} \) is mentioned charge transported to the output - switching transistor in SC CMFB circuit. This circuit was designed as a part of SC CMFB circuit as a "bootstrap" [2].

![Fig. 5. Topology of clock-boost circuit](image)

C. Switched-capacitor CMFB circuit

Fig. 6 shows the topology of the SC CMFB circuit. There are three task for CMFB circuit: sensing the common mode outputs \( i_{V_{OUT+}} \) and \( i_{V_{OUT-}} \) from fully differential OTA, comparison of the sensed results with a reference voltage \( V_{CM} \) (in this design, the reference voltage for CMFB circuit is equal to \( V_{DD} \)) and return the bias voltage \( V_{BIAS} \) back to the OTA by CMFB output. This SC CMFB circuit is clocked by non-overlapping pulses with frequency \( f_{sw} = 20 \ MHz \). These pulses are shifted up in "bootstrap" circuits for better gate-switching of all the
transistors in the Fig. 6. All the transistors have been designed with the same dimensions as a switches with a low enough $R_{ON}$ parameter. The capacitors $cm\_C_1$ ($cm\_C_2$) and $cm\_C_3$ ($cm\_C_4$) have been designed with a specific ratio $k$:

$$k = \frac{cm\_C_1}{cm\_C_3} = \frac{cm\_C_2}{cm\_C_4}$$

(5)

In order to obtain low value of output offset, the specific ratio capacitors $cm\_C_1$ ($cm\_C_2$) and $cm\_C_3$ ($cm\_C_4$) should be perfectly set. However, $cm\_C_1$ and $cm\_C_2$ cannot be too large, because OTA will not be able to drive them. On the contrary, $cm\_C_3$ and $cm\_C_4$ cannot be too small, because the parasitic capacitance of the switching transistors will start to affect the circuit. Transistors $cm\_M_{P1}$, $cm\_M_{P2}$, $cm\_M_{N9}$ and $cm\_M_{N10}$ form the output invertors for driving the SC CMFB outputs. These outputs are connected to the OTA, as it is shown in the Fig. 2 and Fig. 3.

$$C_{sw} \propto \frac{1}{f_{sw}.R_{eq}}$$

(6)

$$A_{INT\_MAX} \propto \frac{i\_C_{S1}}{i\_C_{S3}}$$

(7)

$$f_{cutoff} = \frac{1}{2\pi.\frac{i\_C_{1}.R_{eq}(i\_C_{S3})}{}}$$

(8)

III. ACHIEVED RESULTS

The integrator has been simulated with the signals of varying frequencies, amplitudes and types. For DC simulation of the OTA (with disconnected SC CMFB circuit), the input voltage was swept in the range of $GND$ and $V_{DD}$. In the AC simulation, two periodic sources with $180^\circ$ phase shift were used for simulate differential input signal. Because of using clocks, periodic steady-state analysis (PSS analysis) and periodic AC analysis (PAC analysis) was used. In the Fig. 7 are shown the transfer responses of inverting and non-inverting outputs, where $R\_R\_output$ voltage range can be obtained. Fig. 8 shows frequency response of OTA with maximum gain of $A_{OTA\_MAX} = 46.16$ dB. Bandwidth of proposed OTA is $BW_{OTA} = 24.23$ kHz, while gain-bandwidth is $GBW = 5.03$ MHz.

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(8)
All the essential achieved parameters are summarized in the Tab. 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>0.6 V</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$A_{OTA,\text{MAX}}$</td>
<td>46.16 dB</td>
</tr>
<tr>
<td>$BW_{OTA}$</td>
<td>24.23 kHz</td>
</tr>
<tr>
<td>$GBW_{OTA}$</td>
<td>5.03 MHz</td>
</tr>
<tr>
<td>$P_{M,OTA}$</td>
<td>81.53°</td>
</tr>
<tr>
<td>$A_{INT,\text{MAX}}$</td>
<td>24.09 dB</td>
</tr>
<tr>
<td>$BW_{INT}$</td>
<td>165.95 kHz</td>
</tr>
<tr>
<td>$GBW_{INT}$</td>
<td>1.43 MHz</td>
</tr>
<tr>
<td>$P_{INT}$</td>
<td>22.16 $\mu$W</td>
</tr>
</tbody>
</table>

In addition, interesting thing is the effect of the dimensions of transistor to shape of the switched signal. In the Fig. 12 is the signal switched by NMOS transistor of small dimensions.

In the Fig. 13 is this signal switched by NMOS transistor with the same width as in the Fig. 12, but with increased length.

In the Fig. 14 is this signal switched by NMOS transistor with the same length as in the Fig. 12, but with increased width.

### IV. CONCLUSION

Ultra low-voltage RtR fully differential switched-capacitor filter with supply voltage of 0.6 V was designed for load capacitance $10$ pF. Power consumption of this circuit is 22.16 $\mu$W. If necessary, gain of the integrator 24.09 dB can be increased by larger ratio of capacitors $i_{C_{S1}}$ and $i_{C_{S3}}$. It is important to note, that for possibly increase the gain, it is necessary to design output stages of OTA for higher current values.

This switched-capacitor integrator will be used as the main part of currently designing Sigma-Delta analog to digital converter. Mentioned converter will be developed for energy-harvesting applications (solar panels, wind power stations etc.).

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