Efficiency-Oriented Comparison of Modulation Strategies of a Multi-Output ZVS Resonant Inverter for Domestic Induction Heating

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***Abstract*— Recent developments in domestic induction heating, such as the increase of the cooktop surface flexibility, lead to the design of new multi-output topologies. Those topologies enable the use of several modulation strategies that have to be considered in order to ensure high efficiency while achieving a satisfactory user experience. This paper presents a power losses model of a multiple-output ZVS resonant inverter in order to evaluate the different modulation strategies. This comparison is not only performed from the overall efficiency point of view, but also, considering the discrete losses of each of the power devices. The simulation results have been validated by means of an experimental 3600-W prototype with three induction heating coils of 2000-W rated power.**

Keywords—Induction heating, Induction cooktops, Power losses

I. Introduction

Current design trends on induction heating cooktops evolve towards more flexible surfaces that allow the usage of any pot, with any shape, placed anywhere over the appliance [1]. This relies on the design of cost-effective multi-output power converters and the development of versatile modulation strategies in order to power the multi-coil structures. One of the main constraints of these new designs is the power losses in the semiconductor devices, which are greatly influenced by the component selection and their modulation strategy. These power losses not only affect the overall efficiency of the appliance but also have to be taken into account in the thermal management of the commercial cooktop.

In this paper, a power losses model for the different power devices of a multi-output ZVS resonant inverter is proposed. The proposed power losses model is used to evaluate different modulation strategies and it allows to compare the overall efficiency of the topology and the different sharing of the power losses among the power devices.

II. Topology Description and Modulations

The selected topology is a unidimensional variant of the multi-output ZVS resonant inverter proposed in [2] (Fig. 1). The proposed converter topology enables independent control of the loads. The configurable modulation parameters to set each IH load output power can be seen in Fig. 2.

The output power of the active loads is controlled by the modulation parameters of the high side transistor gate signal, $v_{G,SH}$, i.e. the switching frequency, f_{sw}, and duty cycle, D. Additionally, an enhanced power controllability is achieved by adjusting individually the low-side transistors gate signals, $v_{G,SLi}$. By varying the activation delay, α_i, and pulse width, φ_i, non-complementary transistor activation is generated, as

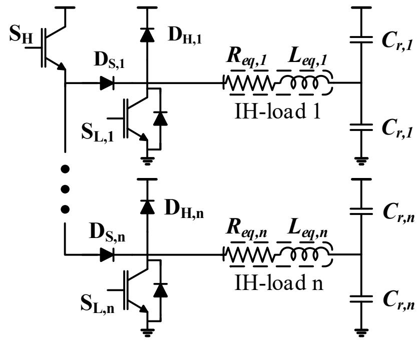

Fig. 1. Unidimensional multi-output ZVS resonant inverter.

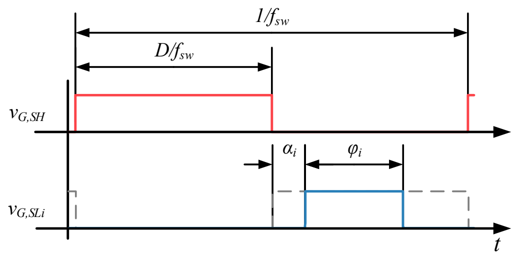

Fig. 2. General scheme of transistor gating signals and main modulation control parameters.

presented in [3]. As a consequence, it is possible to set the desired output power by varying a single parameter, but the parameter selection has implications in the inverter efficiency and power losses share among the different devices.

Therefore, a simulation model of the presented topology has been built in order to obtain the necessary magnitudes to calculate the losses of the different devices.

III. Power Losses Model

The power loss contribution of each of the power devices is calculated from the parameters provided by the manufacturers in the data sheets [4].

IGBT losses, P_{IGBT}, are calculated as the sum of conduction losses, $P_{IGBT,on}$, and switching losses, $P_{IGBT,sw}$.

$$P_{IGBT} = P_{IGBT,on} + P_{IGBT,sw} \tag{1}$$

Conduction losses are the consequence of the non-zero on-state voltage drop. It can be approximated by

$$P_{IGBT,on} = V_{CE,on} I_{C,AVG} + R_{DS,on} I_{C,RMS}^{2}, \tag{2}$$

being $I_{C,AVG}$ and $I_{C,RMS}$ the IGBT collector currents obtained by simulation and dependent on the modulation parameters

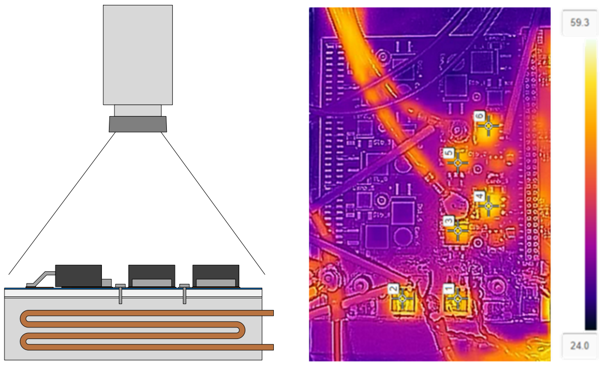

Fig. 3. Test setup schematic and thermal image of the prototype while delivering 3600 W evenly shared between 2 IH loads. Label 1 and 2 are the high-side IGBT, $S_{H,1}$ and $S_{H,2}$, 3 and 4 the series diode, $D_{S,1}$, and the low-side IGBT, $S_{L,1}$, of the cell 1, and 5 and 6 the series diode, $D_{S,2}$, and the low-side IGBT , $S_{L,2}$, of the cell 2.

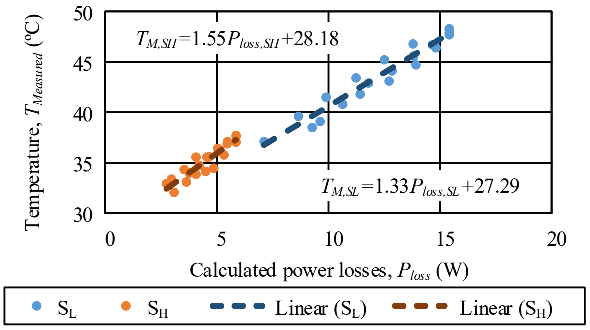

Fig. 4. Linear dependences between the estimated power losses and the measured temperature.

selected, and $V_{CE,on}$ and $R_{DS,on}$ the collector-emitter voltage drop and the channel resistance respectively, obtained from the datasheet curves.

Switching losses are calculated based on the datasheet curves

$$P_{IGBT,sw} = \left(E_{on}\left(I_{C,on}\right) + E_{off}\left(I_{C,off}\right)\right) f_{sw}, \tag{3}$$

where E_{on} and E_{off} the turn-on and turn-off energy losses provided by the manufacturer as a function of $I_{C,on}$ and $I_{C,off}$, which are the collector current in the turn-on and turn-off transition respectively, dependent on the modulation strategy.

IV. Experimental Verification

The experimental verification of the power losses model is done by measuring the temperature of the devices [5]. Based on the thermal-resistance approximation, and assuming constant heatsink temperature, $T_{Heatsink}$, the measured temperature can be approximated as

$$T_{Measured} = P_{loss} R_{eq} + T_{Heatsink} \tag{4}$$

In order to verify the power losses model, an experimental setup is built. The power topology prototype to use in the experimental setup is based on the presented topology and comprises, integrated in a IMS board, two parallel IGBT as the high side transistor, S_H (IGB50N65S5), and 3 low side cells composed by a low side transistor, $S_{L,i}$ (IKB40N65ES5), a series diode, $D_{S,i}$ (DSEI36-06AS), and an antiparallel diode, $D_{H,i}$ (VS-15EWX06FN-M3). This prototype is mounted over a cold plate that works as the heatsink temperature reference.

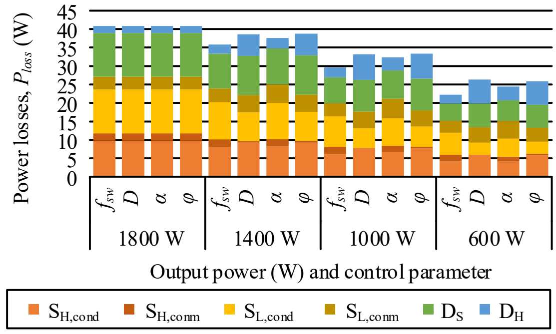

Fig. 5. Comparison of the total losses and the power losses sharing among devices for different power levels and different modulation parameter modification. $S_{H,cond}$ and $S_{H,conm}$ are the sum of the losses of both transistors.

A schematic of the test setup and a capture of the thermal performance can be seen in Fig. 3.

The verification of the power losses model is done by modulating the prototype with a single active load and single parameter variation. The correlation between the calculated power losses and the measured temperature can be seen in Fig. 4. The differences in reference temperature, which is 28 ºC, may be due to the no consideration of the different devices temperature influence on the power losses.

V. Conclusions

In this paper, a power losses model of a multi-output resonant inverter has been proposed and validated through thermography. This model allows efficiency comparison of the different modulation strategies depending on the control parameters (Fig. 5). Square waveform with f_{sw} variation is the most efficient modulation strategy while α_i parameter allows independent power control with lower power losses. Additionally, the individualized power device losses calculation improves the device and packaging selection.

Acknowledgement

This work was supported in part by the Spanish MICINN and AEI under Project PID2019-103939RB-I00, co-funded by EU through FEDER program, by the DGAFSE, by the MECD under the FPU grant FPU17/01442, and by the BSH Home Appliances Group.

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