Floating Voltage Sensing Based on Ceramic Capacitor Ferroelectric Derating

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***Abstract*—This paper presents methods allowing to provide galvanically isolated DC voltage measurement with nearly infinite input impedance. Measurement is based on a ferroelectric effect, creating hysteretic capacitance vs. bias-voltage (C-V) dependence of the ordinary multilayer ceramic capacitors. Voltage measurement is based on AC impedance sensing of a high-density multilayer ceramic capacitor and comparing with ground-referred matched capacitor with corresponding DC bias voltage. Corresponding DC bias voltage is provided by negative impedance converter and a feedback network. Despite finite accuracy (~1%), voltage sensing performed by a capacitor can be advantageous as it allows to implement AC (high-voltage) coupling, and presents nearly ideal infinite input impedance. This can be beneficial in a variety of applications *e.g.* in power management systems, energy harvesting applications, or scientific instrumentation.**

Keywords*—*Capacitor derating, ferroelectric effect, capacitor hysteresis, isolated voltage measurement, multilayer ceramic capacitors (MLCC)

I. Introduction

Measurement of a floating differential voltage source is a common task in many applications. It is required either due to the safety requirements (high-voltage isolation), or system requirements to eliminate high DC voltage or DC ground current between different circuit blocks. For example, voltage sensing in power electronic is often required to provide monitoring of the floating voltages, or monitoring safety operation area (SOA) [1].

Many remote sensor applications with ultra-low power consumption (*e.g.* powered from the energy harvesting) require time-to-time measurement of the supply voltage, without discharging the precious voltage source. Similarly, applications that require monitoring of the voltage on a floating basis without DC current path between DUT and GND are often required in the scientific instrumentation [2].

Differential voltage measurements use variety of techniques, namely based on the operational amplifiers, industrial amplifiers, isolation transformers or optocouplers. Most frequently used structure of the floating voltage sensing is based on a differential amplifier shown in a basic example in *Fig. 1* [3], [4]. This circuit provides the output voltage of:

$$V_{OUT} = -\frac{R_2}{R_1} V_{DIFF} \quad (1)$$

Although circuit offers very high accuracy, input impedance, galvanic isolation and common-mode voltage rage are limited. As highlighted in *Fig. 1* inset, the common mode voltage range is limited by voltage supply range and

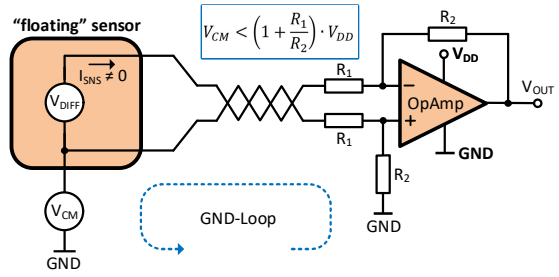

Fig. 1. Measurement system with differential and common mode voltages based on a non-isolated differential amplifier

sensing gain (1), whereas value of the input impedance is the consequence of R_1 resistors' values.

A solution providing simultaneously galvanic isolation and high input impedance is the industrial isolation amplifiers shown in *Fig. 2 a)* and *b)*. Typically, these amplifiers use optical, inductive, or capacitive coupling between voltage sensing and signal domains. However, implementation of these amplifiers requires high density integration and is generally provided at module level [4].

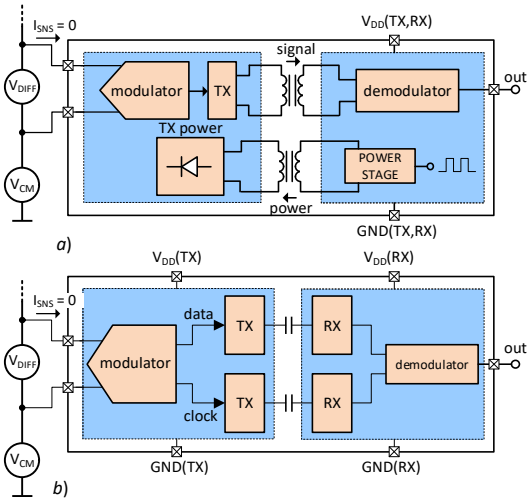

Fig. 2. a) inductive and b) capacitive coupled isolation amplifier providing galvanic isolation and high measuring input impedance.

In this paper, alternative experimental concept of the floating and very high impedance voltage measurement, based on ferroelectric effect encountered in high-density multilayer ceramic capacitors (MLCC), is described. The paper also presents an experimental result showing decent 1% linearity and accuracy with up to 200V common-mode isolation capability corresponding to maximum rated voltage of coupling capacitors.

This paper is organized as follows: in the next section, the capacitance ferroelectric effect is briefly described. *Section III* introduces the concept of the capacitive sensing circuit including the feedback loop. The last *section IV* presents results obtained by measurements on a PCB prototype.

II. Ceramin Capacitor Ferroelectric Effect

Ferroelectric effect of the so called "class 2" capacitors having dielectric with a higher permittivity, and therefore better volumetric efficiency, is often referred to as capacitor derating [5]. It consists in the dependency of capacitance *vs*. applied DC bias voltage. This signifies that capacitance measured by applying AC voltage with small amplitude is a function of the large DC bias voltage.

Typically, class–2 ceramic capacitors are derived from barium titanate $BaTiO_3$. Molecules of the barium titanate in electrically neutral environment have cubical structure and are spatially and electrically symmetrical. In weak electric field, the neutral electric dipoles are randomly oriented, leading to spontaneous polarization. At this condition, permittivity is very high, reaching values up to 10×10^3F/m. Under electric field, neutral cubic crystalline structure undergoes spatial deformation, resulting in the electrical polarization of the molecule. The electrically polarized dipoles start to be more and more aligned with increasing electric field, transforming the molecular structure from rectangular to tetragonal shape. The dielectric with increased polarization exhibits lower relative permittivity ε_r, and thus creates important capacitance drop.

It follows, that dielectric polarization depends on the applied electric field strength E. For given DC voltage, thicker dielectric means that the electric field is weaker, thus less affecting the electric dipoles. It follows that for maximizing the voltage derating effect, low voltage range ceramic capacitors in smaller package are preferred. As example *C-V* characteristics of 100nF set of X7R capacitors for different package size are shown in *Fig. 3* [6].

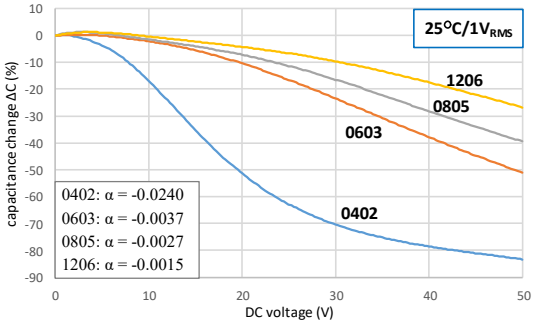

Fig. 3. Example of the C-V characteristic for 100nF X7R capacitors in different SMD package ($1V_{AC}$, 300°K).

Unfortunately, *C-V* characteristic of capacitors with ferroelectric dielectric presents non-negligible hysteresis below critical Currie temperature T_C [5]. This hysteresis is more pronounced at lower temperatures. It can be lowered by decreasing the maximum allowed capacitor voltage but cannot be cancelled. Measured example of *C-V* characteristic of the capacitor used in the prototype presented *section III* is shown in *Fig. 4*.

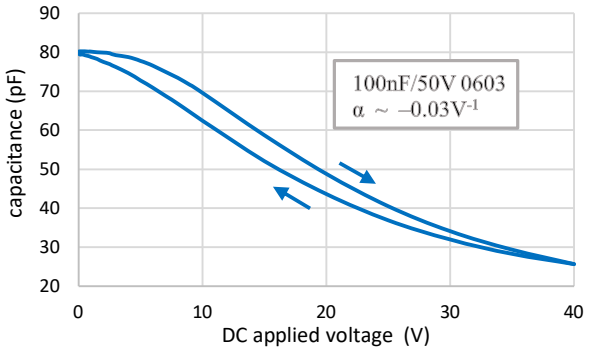

Fig. 4. Measured DC hysteretic C-V curve of sense and reference 100nF/50V X7R capacitors used in the PCB prototype presented in section III.

As it will be shown later by measurement, the hysteresis is well-matched between two capacitors, and optimized feedback-loop allows to perform good tracking of the measurement voltage, resulting in the well-matched results of the reading.

It is to be noted, that capacitor derating is a symmetrical effect [5]. This means that the capacitance change appears identical for both polarities of applied DC bias voltage. Although the symmetry was verified by measurement, precaution was made to implement the sensing and reference capacitors always in the same direction with respect to the original capacitor packaging.

III. Floating Voltage Sensing Method

C-V characteristic of class-2 ceramic capacitors can be used for measurement of the floating or arbitrary common-mode voltage source V_{DIFF}. Measurement setup discussed in this paper is shown in *Fig. 5*. This schematic is composed of measured and common-mode voltage sources V_{DIFF} and V_{CM}, matched sense and reference capacitors C_{SNS} and C_{REF}, coupling capacitors $C_{HV(A,B)}$, sensing high-value resistors $R_{SNS(H,L)}$, and AC source coupling capacitor C_{AC} providing measurement current. AC voltage in the node (A) produces currents in the left and right branches $i_{sns}(t)$ and $i_{ref}(t)$. These currents are given by the node voltage V_A, and values of the left and right capacitances $C_{(L)}$ and $C_{(R)}$:

$$C_{(L)} = \frac{C_{SNS}C_{HV(A)}}{C_{SNS}+C_{HV(A)}},\quad C_{(R)} = \frac{C_{SNS}C_{HV(B)}}{C_{SNS}+C_{HV(B)}} \qquad (2)$$

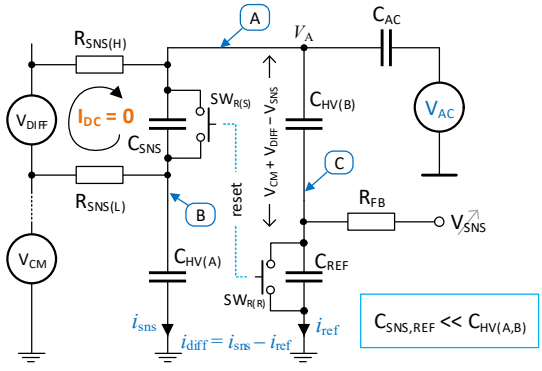

Fig. 5. Voltage sensing with input differential voltage V_{DIFF}, common mode voltage V_{CM}, AC stimuli V_{AC}, and capacitive and resistive coupling. Time-to-time reset is required to reinitialize capacitor hysteretic trajectory.

As the capacitors C_{SNS} and C_{REF}, but also eventually $C_{HV(A)}$, $C_{HV(B)}$, are DC bias sensitive, AC currents $i_{sns}(t)$ and $i_{ref}(t)$ are modulated by their respective DC bias voltages. Considering matched zero-bias values $C_{SNS(0)} = C_{REF(0)}$, and $C_{HV(A,0)} = C_{HV(B,0)}$ and their respective derating characteristics, applying equal input and feedback voltages $V_{DIFF} = V_{SNS}$ leads to the symmetry of the left and right capacitances $C_{(L)} = C_{(R)}$. This symmetry yields equal sense and reference AC currents:

$$i_{sns} = i_{ref} \tag{5}$$

However, deeper analysis of condition $i_{sns} = i_{ref}$ reveals that second solution can be reached by different voltage V_{DIFF}. This 2nd (unwanted) solution act as unstable manifold (repelled).

Unequal voltages $V_{DIFF} \neq V_{REF}$ create current difference:

$$i_{diff} = i_{sns} - i_{ref} = V_A \cdot j\omega\left(C_{(L)} - C_{(R)}\right) \tag{6}$$

This current difference i_{diff} can be measured by a differential analog sensing circuit.

A. Topology of the Voltage Sensing Circuit

An example of the voltage measurement is shown in Fig. 6. Here, measured voltage is connected *via* large coupling resistances to C_{SNS}, which is placed in the vicinity of the reference capacitor C_{REF}. This allows to provide good temperature matching. AC current balancing circuit generates an error signal i_{diff} (6) proportional to $C_{(L)} - C_{(R)}$. This signal is processed by a phase discriminator (synchronous rectifier) and feedback controller. In steady-state, feedback voltage V_{DIFF} corresponds to the measured voltage V_{SNS}.

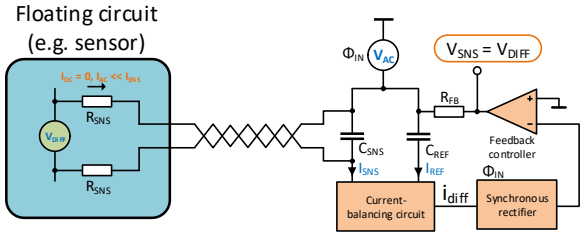

Fig. 6. Simplified capacitance voltage sensing circuit measuring the differential voltage V_{DIFF} of the floating sensor. The output sensed voltage V_{SNS} is applied to the reference capacitor C_{REF}.

In simplified circuit *Fig. 6*, large sense resistances ensure that no parasitic AC current (noise, 50Hz ripple etc.) is added to I_{SNS}. Their values, and eventual additional AC filtering may be considered with respect to the source topology. Generally, I_{AC} much lower that AC current I_{SNS} is required.

B. Current Balancing Circuit

Various circuits providing signal proportional to i_{diff} (6) can be used. Ref. [7] presents circuit of the Negative Impedance Convertor NIC providing signal proportional to the difference ΔC of two matched capacitors $C_0 \pm \Delta C$. As shown in *Fig. 7*, negative impedance convertor is a two-ports circuit creating negative image of the impedance connected to the opposite input port. Consequently, parallel connection of positive and negative capacitance results in cancellation of the constant zero-bias term C_0. Remaining capacitance $2 \cdot \Delta C$ is related to the deviation from the regulation target $i_{sns} = i_{ref}$ and can be measured by a transimpedance amplifier.

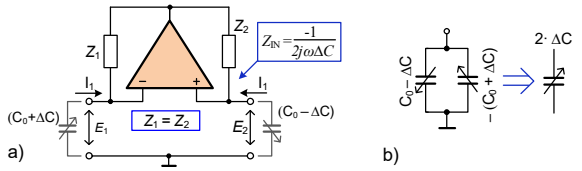

Fig. 7. a) negative impedance converter circuit with operational amplifier [7], b) equivalent parallel connection of positive and negative capacitors

C. Feedback-Loop

AC current i_{diff} related to error capacitance ΔC can be converted to AC voltage V_{OUT} by the capacitive transimpedance amplifier.

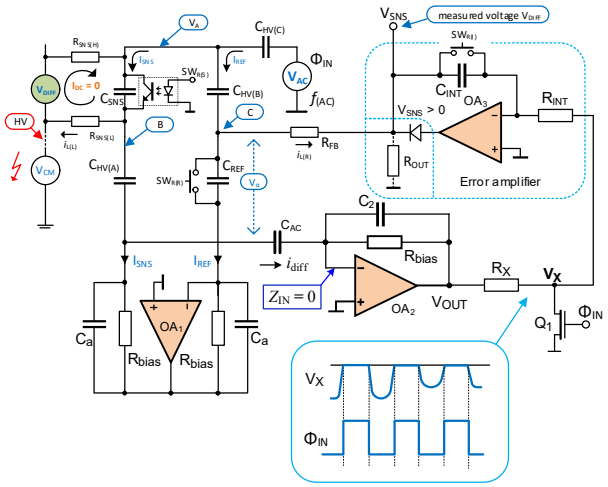

Fig. 8. Circuit of floating voltage measurement with feedback-loop providing $V_{SNS} = V_{DIFF}$ by adjusting reference capacitor DC voltage. Hysteresis reset switches on C_{SNS}, C_{REF} and on the integrator capacitor C_{INT} allows to reinitialize the trajectory on the nonlinear hysteretic C-V characteristic.

As shown on the example of feedback system in *Fig. 8*, transimpedance amplifier is realized by OA_2. For $C_{AC} >> \Delta C$ output voltage V_{OUT} can be written as:

$$V_{OUT} = \frac{sR_b\left(C_{(R)} - C_{(L)}\right)}{sR_bC_2 + 1} \cdot V_A \cong \frac{C_{(R)} - C_{(L)}}{C_2} \cdot V_A \tag{7}$$

As results from (6), current i_{diff} reaches either 0º or 180º phase with respect to the input stimuli V_{AC}. Phase polarity depends on the signum of the difference $V_{DIFF} - V_{SNS}$. In order to extract the polarity of the output voltage (7), AC voltage V_{OUT} is rectified by a synchronous rectifier R_X-Q_1. This synchronous rectifier is gated by the signal Φ_1, being in phase with the input AC source stimuli V_{AC}. In this way, only a half period of V_{OUT} is transmitted to the rectifier output.

Rectified half-wave voltage is integrated by an integrator implemented by OA_3 shown in *Fig. 8*. As the voltage derating is symmetrical, a diode is added to the operational amplifier output. This diode avoids the OA_3 output to initiate negative regulation trajectory This would result in wrong result and premature saturation of the feedback loop.

In the simplified schematic shown in *Fig. 8*, an optocoupler switch and additional switches $SW_{R(R)}$ and $SW_{R(S)}$ are added. The purpose of these switches is to provide a periodical reset of the sense and reference capacitors. This allows to reinitialize the capacitor's voltage trajectory and thus cancel the hysteresis. In case the coupling capacitors $C_{HV(A)}$ and

$C_{HV(B)}$ also present hysteretic behavior, similar periodic reset should be performed.

Dynamic behavior of the sensor can be sufficiently approximated by 1st order lag transfer function, and the stability can be easily guaranteed. On the other hand, detailed analysis allows to better optimize the circuit accuracy and time response. In particular, smooth and non-resonant time response is essential for accurate tracking of the C_{SNS} capacitor voltage. This allows to attenuate the error from the hysteresis and relax the requirement on capacitor reset.

IV. Implementation Results

Circuit prototype was implemented on a test PCB, and electric performances were measured in wide voltage range. In order to provide high sensitivity of measurement, X7R 0603 100nF/50V sensing capacitors with *C–V* characteristic shown in *Fig. 4,* and coupling capacitors C_{HV} = 1µF/630V were used in the prototype. Capacitors C_{SNS} and C_{REF} were preselected to have zero-bias capacitance in range < ±5%.

Negative impedance convertor and error amplifier were built with TL082 operational amplifier. Sinewave 3kHz/1V_{peak} AC input voltage have been used to generate reference and sense currents i_{ref} and i_{sns}. An example of the AC stimuli V_{AC}, rectified voltage V_X and the phase signal Φ_1 during the V_{DIFF} voltage step is shown in *Fig. 9*.

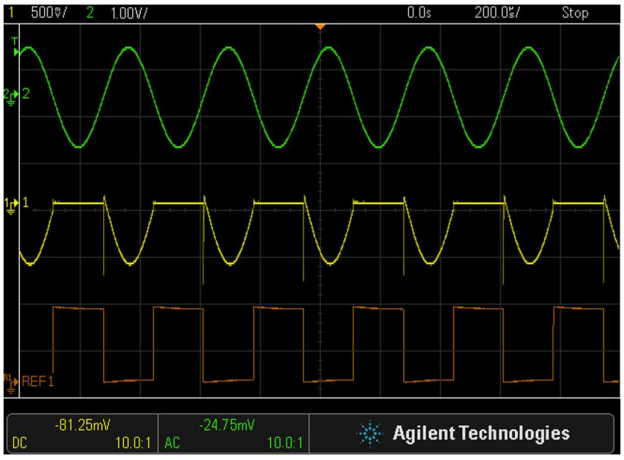

Fig. 9. Captured waveforms of the input sinewave stimuli of 2V_{pp}, rectified signal V_X and phase signal *Φ*.

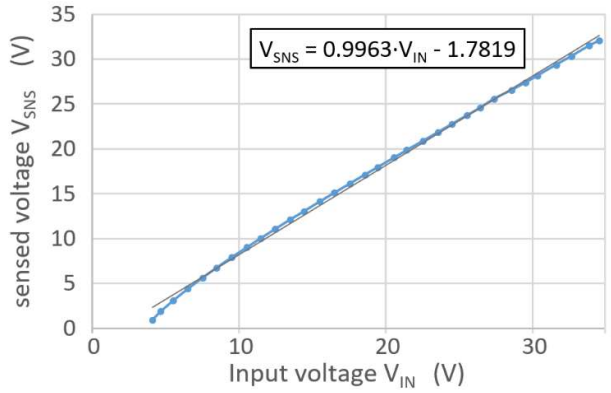

Fig. 10. DC transfer characteristic V_{SNS}/V_{DIFF} for positive common mode voltage V_{CM} = 34V.

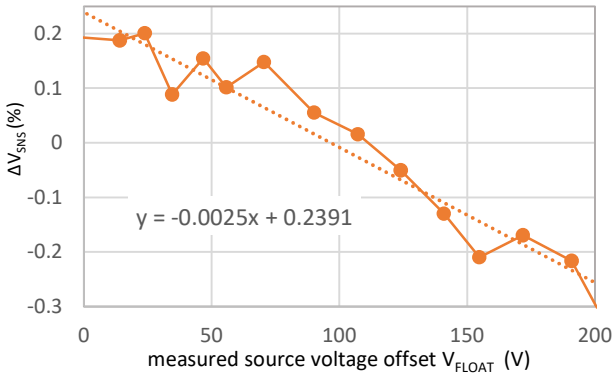

Fig. 11. Common mode error for V_{diff} =10V.

Main outcome of the measurement is the DC transfer characteristic V_{SNS}/V_{DIFF} shown in *Fig. 10*. This transfer characteristic was measured for common-mode voltages +34V. Measurement exhibits negligible gain error and stable offset voltage.

Common-mode voltage sensitivity for constant input voltage V_{DIFF} = 10V was measured in range of 0÷200V and is shown in *Fig. 11*. The error remains below 0.3%, and it is mainly originated from the mismatch of the high-voltage coupling capacitors.

The circuit was measured across a wide temperature range, and the output voltage thermal dependency error was approximately 0.05%/ºK. It is also to be noted, that microphonic effect was observed during the measurement.

Conclusion

This paper describes a concept study of isolated absolute-value voltage measurement, based on the ferroelectric effect of multilayer class-2 ceramic capacitors. The presented circuit contains negative impedance convertor and simple feedback loop controller, providing output voltage equal to measured differential voltage. Measurement results reach decent performances as the linearity and offset voltage. Focus of next work will be to explore inconvenient hysteretic behavior, understanding statistical matching of the C-V characteristic between different capacitors, and optimization of the feedback loop.

References

[1] K. Schon, "High Voltage Measurement Techniques: Fundamentals, Measuring Instruments, and Measuring Methods," *Book,* Springer 1st ed. 2019 Edition.

[2] Nagel, J. H. "Biopotential Amplifiers." *The Biomedical Engineering Handbook*: Second Edition. Ed. Joseph D. Bronzino Boca Raton: CRC Press LLC, 2000.

[3] R. Mancini, "Op Amps for everyone" *Design refference SLOD006B Texas Instrument*, 2002, available online.

[4] T. R. Padmanabhan, "Industrial Instrumentation: Principles and Design," *Book*, Springer, 1999.

[5] D. Damjanovic, "Ferroelectric, dielectric and piezoelectric properties of ferroelectric thin films and ceramics ," *Rep. Prog. Phys*. 61 (1998) 1267–1324.

[6] "The Important Points of Multi-layer Ceramic Capacitor Used in Buck Converter circuit," *Rohm semiconductors app. note* 62AN089E.

[7] V. Michal, "Front-end ΔC/C0 capacitive interface based on negative impedance converter," *IET Electronic Letters*, Vol. 50 No. 23, 2014.