Fast Real-Time Data Exchange among Distributed Control System of STATCOM Installation

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***Abstract*— Power installations based on power converters in power transmission and power distribution require real-time control which is usually implementing using multiple control units. Therefore, very fast data exchange within constant sampling periods across whole control system is needed. This paper deals with the development and implementation of a specific communication protocol for an embedded modular control system. The communication protocol employs LVDS bus and it is designed for fast data exchange between master and slave control units. The protocol is used in control system REMCS of a STATCOM of 1.35MVA installed in distribution power grid of 22 kV.**

Keywords—real-time control, LVDS communication protocol, STATCOM

I. Introduction

In the field of power transmission and power distribution, systems with power semiconductor converters such as line voltage conditioners, active power filters compensating harmonic current components or static compensators (STATCOM) compensating reactive power above all are increasingly penetrating to the power grids [1-3]. In these installations, where the rated power range is from tens kVA to tens MVA, the main power semiconductor converter consists of multiple power blocks and its control is usually provided by a distributed control system consisting of several control cards, where important voltage and current control loops are implemented. Fast and reliable data exchange is crucial to ensure the control of such systems.

A very fast data exchange between the control cards is necessary to ensure the real-time control. Typically, this involves the exchange of data of constant size within fixed sampling periods, typically tens of microseconds. The data contains mainly measured analogue quantities (typically measured voltage and current values) as well as control quantities, i.e. outputs of control algorithms (typically PWM duty cycles of power transistors). The fixed sampling period of the control loops limits the communication parameters. In addition to speed, the absence of crosstalk is crucial. In this context, it should be noted that broken data received cannot be repeated because it is not possible to introduce delay to the control loops, because delayed control signals of the power transistors can cause overcurrent and destruction of the power converter.

The development of the STATCOM system designed for 22 kV distribution power grids was the main motivation for the development of a distributed control system (REMCS) and for the implementation of a specific communication protocol. Nowadays there are many verified and well documented protocols /for industrial applications. For example, we can mention low-speed CAN bus, LIN bus or protocols based on industrial Ethernet: Ethernet/IP, Modbus, Pofibus, CANopen, DeviceNet or EtherCat [4].

However, in order to meet the specific requirements of our application such as fast communication within fixed sampling periods, the fixed communication frame, the absence of re-transmission of broken data, etc., we decided to develop and implement our own and open communication protocol.

II. STATCOM for Power Distribution Grids of 22 kV

Fig. 1 shows the final STATCOM installation in the power installation grid of 22 kV. The block scheme of the distributed control system (REMCS) [5, 6] including converter topology is depicted in Fig. 2.

Fig. 1. Final STATCOM installation in distribution power grid of 22 kV

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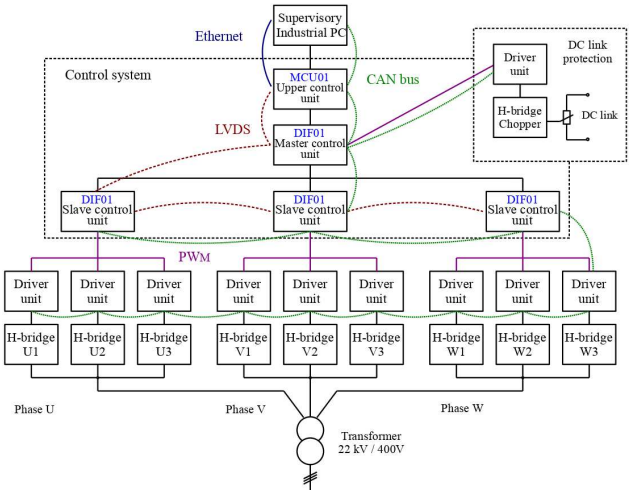

Fig. 2. Block scheme of REMCS.

The power converter is connected to the power grid 22 kV via the three phase transformer 22/0.4 kV. Each phase of the secondary winding of the transformer is supplied by three IGBT-based power blocks of 150 kVA connected in parallel. Each power block is a single phase voltage source inverter (VSI), i.e. full bridge of power transistors. In order to achieve required current, the H-bridge is doubled in each power block, see Fig. 3.

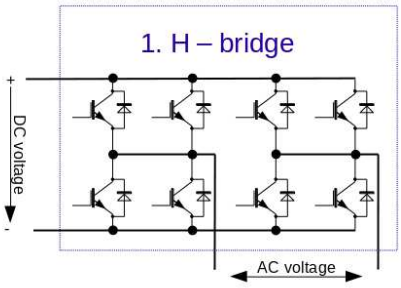

Fig. 3. Single phase voltage source inverter – double H-bridge

Power blocks operates at the dc-link voltage of 730 V and generates the output voltage of 400 V_{rms} on the ac side. The whole installation is built by 9 basic power blocks; the power of the whole STATCOM is 1.35 MVA. In order to achieve high quality of the output current (375 Arms for each basic power block), each H-bridge operates at switching frequency of 9 kHz.

III. Distributed Control System REMCS

It can be seen from the Fig. 2 that the developed STATCOM is rather large installation placing high demands on the control system and signal distribution.

The REMCS modular control system was developed by the Research and Innovation Centre for Electrical Engineering (RICE), Faculty of Electrical Engineering, University of West Bohemia. It is a generic embedded modular control system determined mainly for drive control area. In this application, it consists of five control cards. Three slave control units (DIF01 – direct interface unit, see Fig. 2) with attached binary IO unit are used for control of three phases of the converter (each phase consist of three power blocks). These control cards are used as slave cards in the topology. Their main tasks include AD conversion (voltage and current measurement), data exchange with master card, control of power transistors based on PWM duty cycles received from the master card, and error handling.

The fourth DIF01 control card is used as master control unit (see Fig. 2). It receives data from the slave cards, i.e. measurements across the whole converter. Main voltage and current control loops are implemented here. Based on the measurements, the master card computes PWM duty cycles for power transistors and these are distributed to the slave cards.

Upper control loops are implemented in slave control unit called microprocessor control unit - MCU01, see Fig. 2. This card performs external measurements, mainly voltage and current signals introduced from the distribution substation. Moreover, it collects all the data from the whole converter and transmits the data via the UDP/IP protocol to the supervisory industrial PC (see Fig. 2) which is used for monitoring and data logging above all.

A. Communication Structure of REMCS system

The generic structure of the REMCS card-to-card communication system is illustrated in Fig. 4. It is based on the LVDS/CML physical layer with 10bit transmission coding. The used topology is formed by one communication ring (see Fig. 4) and it is designed to meet requirements of the STATCOM application, which includes fast communication within constant sampling periods (55.6 µs). The effective data transfer rate of the serial line is 1.04Gbps.

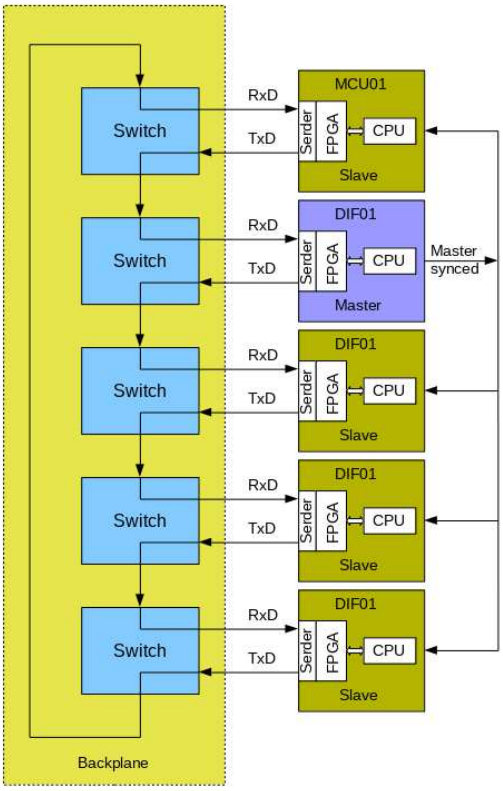

Fig. 4. Communication structure of the REMCS system.

Slave cards (DIF01 slave) of the REMCS system send measured and status data which is called *Card Specific Status data* (CSSD) [7]. In the same time, they receive data sent by the master card (DIF01 master) containing PWM duty cycles, binary outputs and user data. This set of the control data is called *Card Specific Control Data* (CSCD). These datasets can be easily shared between all cards and customized for the

target application. It should be pointed out that all transmitted data are received by the particular card without the microprocessor intervention. Thanks to the receiver implemented in the FPGA (see Fig. 4 and 5), no interrupt of the microprocessor is needed.

B. Application Data

For the purpose of the STATCOM application, following data are exchanged:

- In the beginning of the sampling period, measurements taken by AD converters, error states, and binary inputs are transmitted from all slave cards to the master card.
- Before the end of the sampling period, PWM duty cycles and other application data from the master control unit processing the main control loop are transferred to all slave cards.
- All data sent from the master and slave control units (all DIF01 cards) is read by the MCU01 card, where the upper control loop is implemented. Moreover, the MCU01 provides us with data logging and system monitoring.
- The data shall be transmitted synchronously with the master control loop at sample rate of 18 kHz (55.6 µs).

The inverter control data is distributed to all slave cards. Therefore, their control algorithms are designed with emphasis to the minimum real-time data exchange. To meet the requirement for the synchronous data exchange with the main control loop, modification of the current LVDS communication protocol was needed. As a result, communication latencies are minimal.

C. FPGA and transfer rate

The communication between the FPGA and the microprocessor is performed over a 16-bit parallel bus. Data transfer speed between FPGA and the microprocessor TI TMS570 is the main bottleneck in card-to-card communication. The theoretical reading speed of 12.5 MBps and writing speed of 25 MBps were not achieved. In the final application, writing speed of 22 MBps and reading speed of 11 MBps was achieved for a 64-bit word. Moreover, the speed is lower when using 32-bits words. Based on these speed limits, the LVDS/CML bus topology was modified and simplified as much as possible.

In order to achieve a sufficiently fast data transfer, synchronization of the communication ring (see Fig. 4) is needed. Holding the ring synchronized allows significant reduction in time required for a single communication cycle (for two cards connected to backplane the time to establish the communication is 1.28 µs, for five cards, the time increases to 6.4 µs).

D. Error handling and safety

In case of error detection, all fire signals (PWM outputs) of power modules across the whole converter must be blocked simultaneously and immediately. To do so, a global error HW signal is designed on the backplane. It interconnects all cards and ensures hardware disconnection of all PWM outputs in case of any serious error detected by any card.

In general, the reaction on any error is identical; the whole converter must be blocked to avoid overcurrent in any power module of the STATCOM. Therefore, the global error HW signal is always activated first and all PWM outputs are blocked. Later on, the information about the error cause is transmitted via CAN bus

IV. Communcation Protocol And Data Exchange

A simplified block diagram of the communication between the LVDS bus and the FPGA, and between the FPGA and the microprocessor is shown in Fig. 5. The LVDS serial bus is connected to a SERDES (serializer/deserializer transmitter) circuit that converts serialized LVDS data to a parallel interface suitable for communication with the FPGA. The user data area is written to the corresponding FPGA message area by the microprocessor, before the message is sent. The other data is read from the FPGA memory area. All messages are passed in from master back to master (see Fig. 4). The message sent by the master is stored to the FPGA of the particular slave card. After receiving, the message is replaced by the slave message and it is send via the ring to the master card.

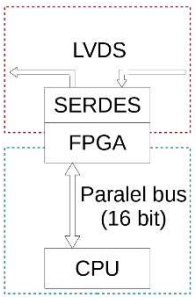

Fig. 5. Connection of FPGA and microprocessor (CPU).

Fig. 6 shows the data transfer and timings between the CPU and FPGA (blue box), and between the FPGA and LVDS (red box). The length of the sampling period is 55.6 µs and it is synchronous with the sampling rate of the AD converters. This ensure that all samples are fetched at the same time. The synchronization signal is generated by the FPGA of the master (step 1, see Fig. 6). This signal is distributed to all slave cards and starts the ADC conversion (3.4 µs). Once the conversion in the master card is completed, the global signal EOC is generated, and distributed to all cards. It triggers an interrupt in all CPUs (step 2), which does not block the communication and data processing.

Inter-process communication in one sampling period is divided into two parts. The first part includes ADC reading, measured and user data transfer (see step 3,4,5 and 9).

First, the master card starts the communication (step 3), then it reads local ADC data (step 4) and finally it reads ADC and user data from the slave cards (step 5). It is guaranteed that the steps 3-5 take 6.4 µs and they are completed before the master application loop is started. Table I summarizes data read by the master in step 5.

Unlike the master, the DIF01 slave cards are ready for the application loop in 1.3 µs. This is because they read user data only, send by the master (step 4). Similarly, the MCU slave card is ready within 2 µs. It reads the user data from the master as well. Unlike the DIF slaves, the MCU reads 16 ADC channels.

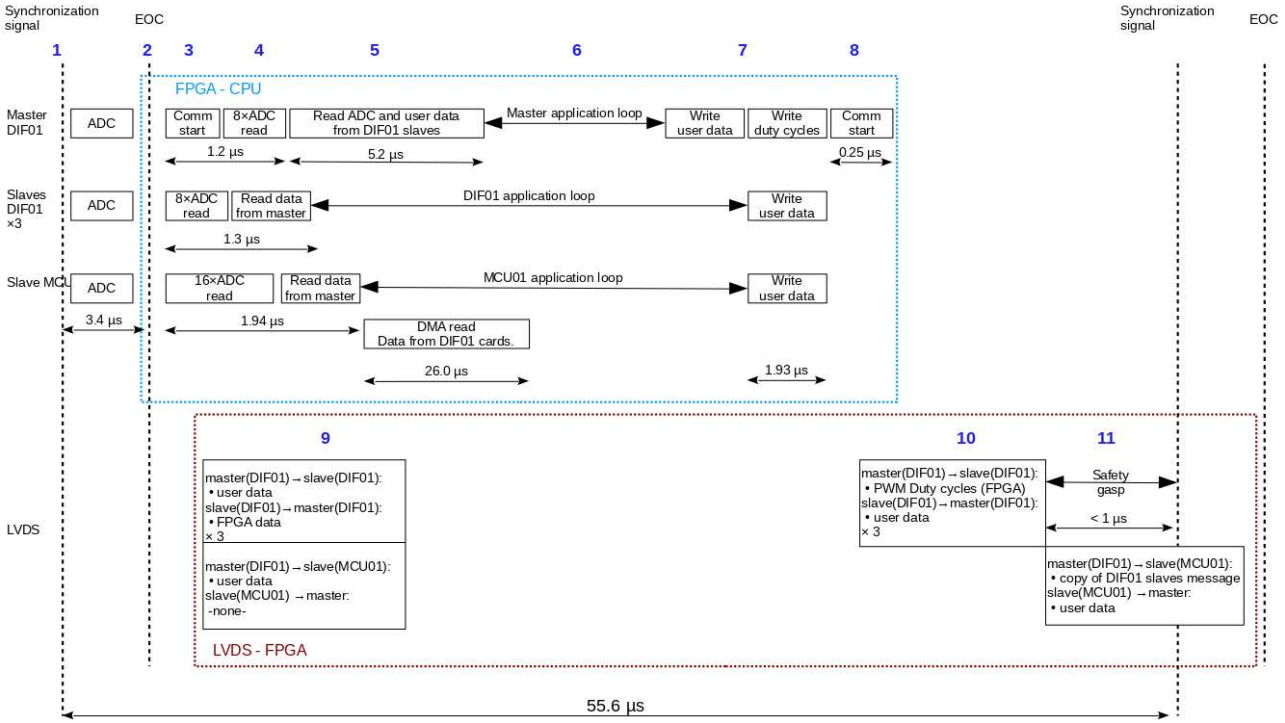

Fig. 6. Block diagram of communication over one sampling period

TABLE I. DATA SENT FROM DIF01 SLAVES TO MASTER.

Index	Bits	Field / Description
0	64	User data
3	16	PLL status
5	96	I/O signals (system, local)
11	8	LED status
12	8	General inputs
13	12	PWM blocking
14	16	Over limits of the analogue inputs
15	6	PWM errors
16	16	Hardware limits of the analogue inputs
17	8 ×16	8 × ADC inputs (raw data)
25	6	PWM binary status (GIO mode)

Thanks to DMA, the MCU can read all the data from all DIF slave cards in the background while processing the application loop (step 6). In addition, the data read via DMA are directly stored to the Ethernet peripheral area. This allows more efficient utilization of the available CPU power. Table II summarizes the data read by MCU using the DMA.

TABLE II. OVERAL DATA PACTED SENDS TO MCU01 CARD.

Index	Bits	Field / Description
0	64	Master user data
4	8 ×16	8 × ADC inputs (raw data) from card U
12	16	PWM status from card U
13	2x16	PWM duty cycles from card U
15	8 ×16	8 × ADC inputs (raw data) from card V
23	16	PWM status from card V
24	2x16	PWM duty cycles from card V
26	8 ×16	8 × ADC inputs (raw data) from card W
34	16	PWM status from card W
35	2x16	PWM duty cycles from card W
37	8 ×16	8 × ADC inputs (raw data) from Master card
45	64	User data to card U from master
49	64	User data to card V from master
53	64	User data to card W from master

After the first part of the inter-process communication is completed, calculation of the application loop is started. (step 6, see Fig 6). Thanks to the communication structure discussed above, constant computation time for the application loop is guaranteed in every particular card. In the end of the master application loop the PWM duty-cycles are calculated. These must be distributed to the DIF slaves. The PWM duty-cycle values and other data (see Table III) is written into appropriate mailboxes (step 7) in the FPGA.

TABLE III. THE MASTER CARD MESSAGE TO THE SLAVE CARD

Index	Bits	Field / Description
0	32	User data
4	32	I/O Signals (local)
6	8	LED control
7	6 ×16	6 × PWM duty cycle

Subsequently, a data transfer between the master and slave cards is initiated from the master card (step 9). The data transfer via the LVDS bus is done without CPU involvement. All slave cards send user data only before the end of the sampling period (step 7).

V. EXPERIMENTAL RESULTS

One of the main tasks of the developed communication protocol is to distribute final PWM duty-cycles across the whole power converter. Fig. 7 shows synchronized PWM signals generated by DIF slave cards. These signals are based on the duty cycles computed by the master card and distributed via the LVDS bus in real time.

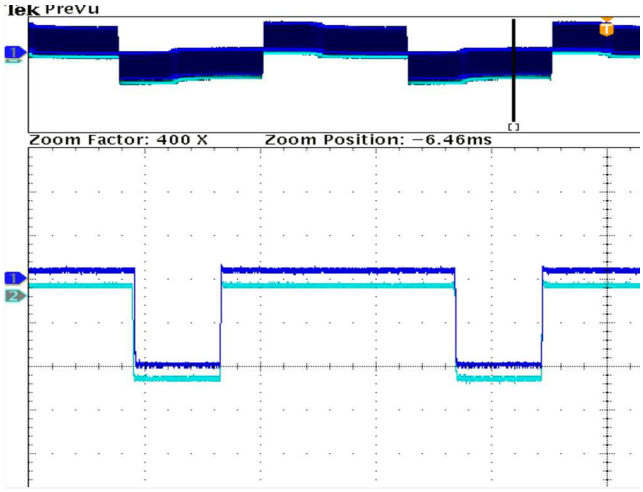

Fig. 7. Synchronous PWM (9 kHz) generated by REMCS (PWM signals of two different H-bridges)

Fig. 8 illustrates three currents generated by three H-bridges connected in parallel which are controlled by synchronized PWM signals.

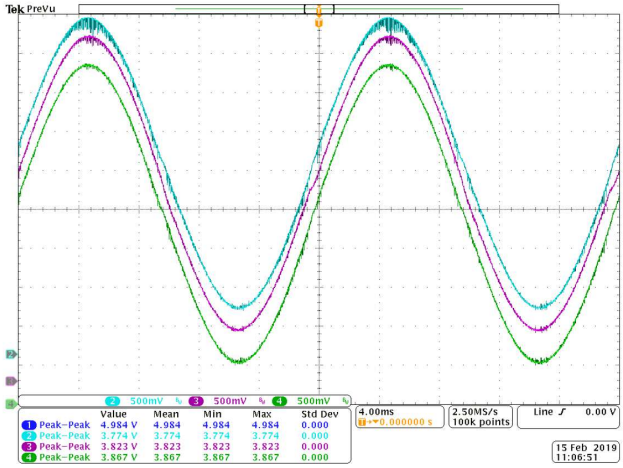

Fig. 8. Currents of H-bridges in converter phase V, the (total output current is 1000 Arms): Ch2: Current of H-bridge V.1 [125 A/div.], Ch3: Current of H-bridge V.2 [125 A/div.], Ch4: Current of H-bridge V.3 [125 A/div.].

VI. Conclusion

The special communication protocol based on the LVDS bus is discussed in this paper. The protocol is designed and developed for rather large installations with power converters used especially in transmission and distribution power grids. These installations usually employ distributed control systems. In the same time the converter control runs in very fast control loops with constant sample rate, where all critical data must be transmitted in real time. In our case, the STATCOM converter is controlled with sampling period of 55.6 µs. This places high demands on data rate, minimum latency and maximum reliability of the communication. Besides others, the developed communication protocol enables to acquire all measurements from slave cards while providing constant time period for computation of the main control loop. Consequently, all PWM duty-cycles computed by the master are distributed among all slave cards which control the power modules. To avoid overcurrent and other dangerous states, precise synchronization and real-time communication without delay is ensured. In addition, the the implemented FPGA IP stacks enable communication via LVDS with minimum CPU involvement.

The reliability of the proposed protocol was verified by two years of operation of the STATCOM with rated power of 1.35 MVA in the medium-voltage distribution power grid.

Acknowledgment

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