

Kerwin-Huelsman-Newcomb Filters Using DVCCs

Jaroslav Koton^{†1}, Norbert Herencsár^{†2}, Kamil Vrba^{†3}, Oguzhan Cicekoglu[‡]

[†]Brno University of Technology, Dept. of Telecommunications, Purkynova 118, 612 00 Brno, Czech Republic
koton@feec.vutbr.cz¹, herencsn@feec.vutbr.cz², vrbak@feec.vutbr.cz³

[‡]Bogazici University, Dept. of Electrical and Electronic Engineering, 34342-Bebek-Istanbul, Turkey
cicekoglu@boun.edu.tr

Abstract – A voltage-mode Kerwin-Huelsman-Newcomb (KHN) filter using DVCCs is presented. The filter has high input impedance and employs four active elements, two grounded capacitors and five grounded resistors. Based on the generalized description of the proposed structure various solutions are presented and compared. Spice simulation results are included to verify and demonstrate the feasibility of the KHN filter.

I. INTRODUCTION

Analog filters are the basic building blocks in electronic circuit applications. The KHN (Kerwin-Huelsman-Newcomb) filter is one of well-known biquads and offers several advantages such as low components spread, low passive and active sensitivity performance, good stability behavior [1]. It provides the high-pass (HP), band-pass (BP), and low-pass (LP) filtering functions simultaneously. The progress in microelectronic area presents new or improves the properties of active elements such as Current Feedback Amplifiers (CFA) [2], Operational Transconductance Amplifiers (OTA) [3], Current Conveyors (CC) [4], or Voltage Conveyors [5]. These active elements are often used for the design of frequency filters and also structures, whose behavior is equivalent to the KHN filter [6]-[10] since these active elements enable to reduce the number of floating passive elements in the structure, which is very suitable for integrated implementation [11].

Recently, a number of new circuit solutions using three and four DVCCs (Differential Voltage Current Conveyor) have been presented [12]-[14]. In this paper we present new structure employing four DVCC and seven grounded passive elements and that supplements the group of KHN equivalent biquads using DVCC. For the analysis the circuit is with advantage described in general to define all possible solutions. To verify the feasibility of the proposed structure Spice simulations are presented, while CMOS structure of the DVCC [14] has been used.

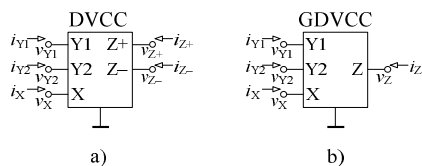


Fig. 1 Circuit symbol of a) DVCC, b) GDVCC.

II. CIRCUIT DESCRIPTION

The DVCC defined in [15] is a five port building block with positive and negative current output (Fig. 1a) that can be described by following hybrid matrix:

$$\begin{bmatrix} v_X \\ i_{Y1} \\ i_{Y2} \\ i_{Z+} \\ i_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_X \\ v_{Y1} \\ v_{Y2} \\ v_{Z+} \\ v_{Z-} \end{bmatrix}. \quad (1)$$

To make the final circuit solution as simple as possible, only single output DVCC is used. If all alternative solutions of the proposed circuit (Fig. 2) are to be found, it is suitable to use a generalized DVCC (GDVCC) (Fig. 1b), where the relationship between port voltages and currents is given as follows:

$$v_X = a_1 \cdot v_{Y1} + a_2 \cdot v_{Y2}, \quad i_Z = c \cdot i_X, \quad (2)$$

where a_1 , a_2 , and c can be of the value +1 or -1, while $a_1 \cdot a_2 = -1$.

General voltage transfer functions of the proposed circuit in Fig. 2 are:

$$\frac{V_{HP}}{V_{IN}} = \frac{s^2 a_{21} c_1 C_1 C_2 G_1}{D}, \quad \frac{V_{BP}}{V_{IN}} = \frac{s a_{21} a_{12} c_1 c_2 C_2 G_1 G_2}{D}, \quad (3a, b)$$

$$\frac{V_{LP}}{V_{IN}} = \frac{a_{21} a_{12} a_{13} c_1 c_2 c_3 G_1 G_2 G_3}{D}, \quad (3c)$$

where

$$D = s^2 C_1 C_2 G_5 - s a_{12} a_{14} c_2 c_4 C_2 G_2 G_4 - a_{11} a_{12} a_{13} c_1 c_2 c_3 G_1 G_2 G_3. \quad (4)$$

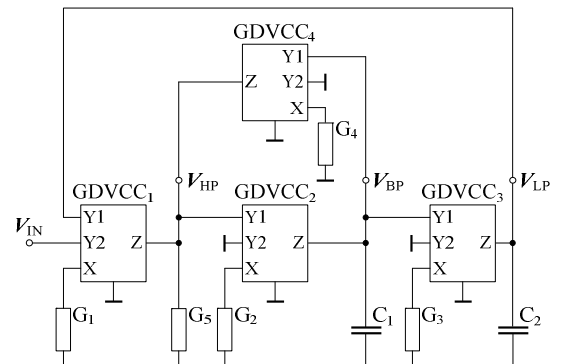


Fig. 2 Proposed generalized circuit.

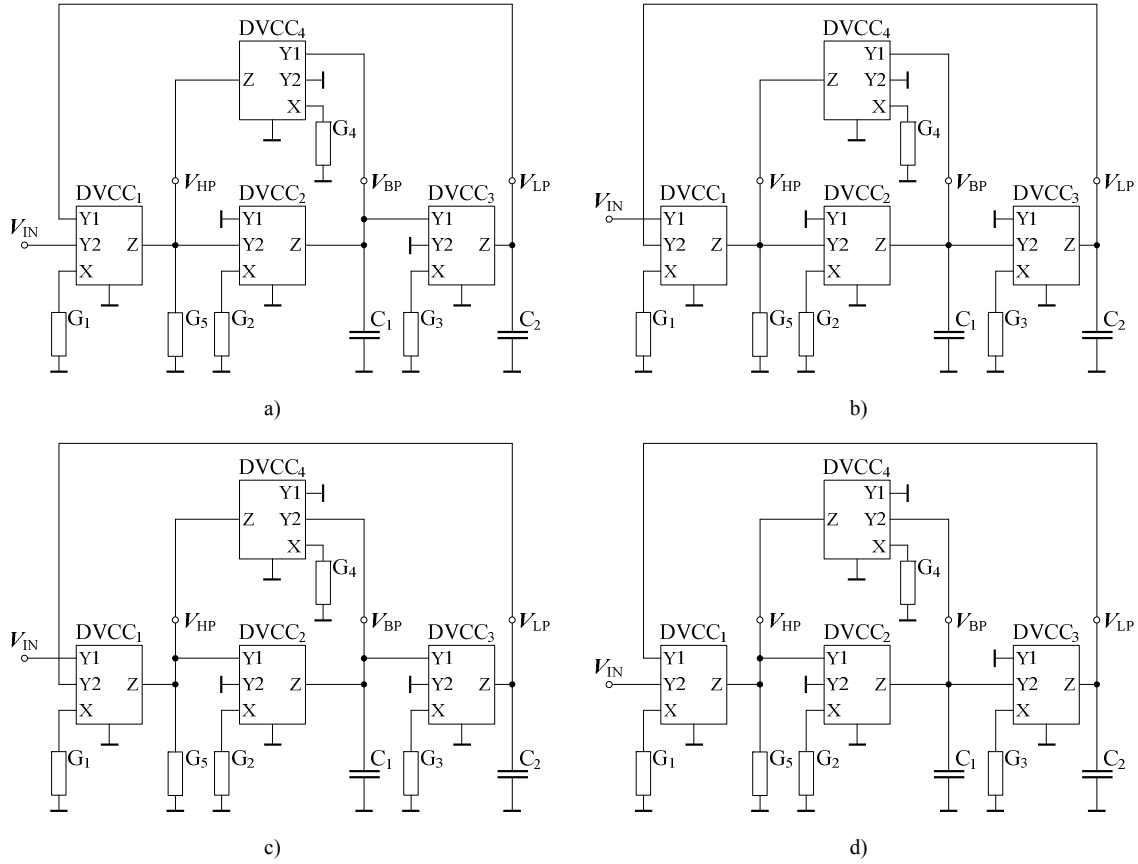


Fig. 3. Alternative solutions of KHN equivalent biquads according to Table I.

Analyzing the denominator of the transfer functions (4) following conditions must be fulfilled to design a stable circuit:

$$a_{12}a_{14}c_2c_4 = -1, \quad a_{11}a_{12}a_{13}c_1c_2c_3 = -1. \quad (5)$$

In this case, 23 combinations of a and c coefficients can be found, while the most suitable are those where $c_1 = c_2 = c_3 = c_4 = 1$, i.e. a DVCC with a positive current output Z is used, which is an advantage in avoiding additional current mirrors in the internal structure to obtain a Z^- . Consequently, the number of possible combinations of the a coefficients reduces to 4 (Table I).

Table I. Coefficients combinations

Solution	a_{11}	a_{12}	a_{13}	a_{14}
A	1	-1	1	1
B	-1	-1	-1	1
C	-1	1	1	-1
D	1	1	-1	-1

The final circuit solutions of the proposed structure are shown in Fig. 3. The angular frequency ω_0 and quality factor Q are given by:

$$\omega_0 = \sqrt{\frac{G_1G_2G_3}{C_1C_2G_5}}, \quad Q = \frac{1}{G_4} \sqrt{\frac{C_1G_1G_3G_5}{C_2G_2}}. \quad (6)$$

The passive sensitivities of the proposed filter

derived from (6) are:

$$S_{G_1, G_2, G_3}^{a_0} = -S_{C_1, C_2, G_5}^{a_0} = \frac{1}{2}, \quad S_{G_4}^{a_0} = 0,$$

$$S_{C_1, G_1, G_3, G_5}^Q = -S_{C_2, G_2}^Q = \frac{1}{2}, \quad S_{G_4}^Q = -1,$$

hence are low and not larger than unity in absolute value.

The design equations for required value of ω_0 and Q are given by taking $C_1 = C_2 = C$, $G_1 = G_5$:

$$G_2 = G_3 = \omega_0 C, \quad G_4 = G_5 / Q. \quad (7)$$

It can be seen that Q is controlled by passive element G_4 or G_5 without affecting ω_0 .

The output voltage polarities of the alternative solutions are given in the Table II. It is seen that adding up the output voltages V_{LP} and V_{HP} in the variant B and C a band-stop (BS) filter can be designed. Similarly, adding up the output voltages V_{LP} , V_{BP} , and V_{HP} in the variant B an all-pass filter can be obtained.

Table II. Output voltage polarities

Solution	V_{LP}	V_{BP}	V_{HP}
A	1	1	-1
B	1	-1	1
C	1	1	1
D	1	-1	-1

III. SIMULATION RESULTS

The behavior and comparison of alternative circuit solutions in Fig.3 have been done by Spice simulations. The used CMOS internal structure of the DVCC with a single positive current output Z is shown in Fig. 4. [14]. As MOS transistor the SCN 05 feature size $0.5 \mu\text{m}$ from MOSIS vendor: AGILENT has been used, while the MOSIS parametric test results can be found in [13]. The transistor aspect ratios are given in Table III [14], and $V_{DD} = 1.5 \text{ V}$, $V_{SS} = -1.5 \text{ V}$, $V_{B1} = V_{B2} = -0.52 \text{ V}$.

The circuits in Fig. 3 were simulated to have $f_0 = 1 \text{ MHz}$ and $Q = 0.707$. The circuits design parameters are $C_1 = C_2 = 10 \text{ pF}$, $R_2 = 1/G_2 = R_3 = 1/G_3 = 15.9 \text{ k}\Omega$, $R_1 = 1/G_1 = R_5 = 1/G_5 = 22.5 \text{ k}\Omega$, $R_4 = 1/G_4 = 15.9 \text{ k}\Omega$. The simulation results of the proposed circuits are shown in Fig. 5.

It is seen that the simulation results agree well with theoretical behavior. Comparing the simulations, the best results are in the case of the variant B and C (Fig. 5b,c), where the most significant difference to other ones is in the low-pass response.

In the Fig. 6 the band-pass magnitude responses of all variants are shown for $f_0 = 1 \text{ MHz}$ and $Q = 10$. The

values of passive elements are $C_1 = C_2 = 10 \text{ pF}$, $R_2 = R_3 = 15.9 \text{ k}\Omega$, $R_1 = R_5 = 1.59 \text{ k}\Omega$, $R_4 = 15.9 \text{ k}\Omega$

Also here the behavior agrees with theoretical assumptions and for all alternative solutions the magnitude response is almost the same.

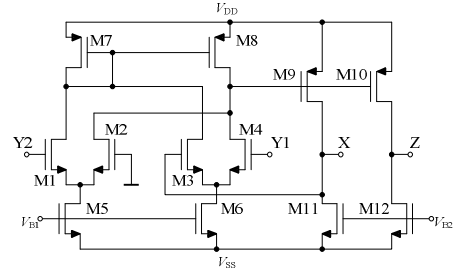
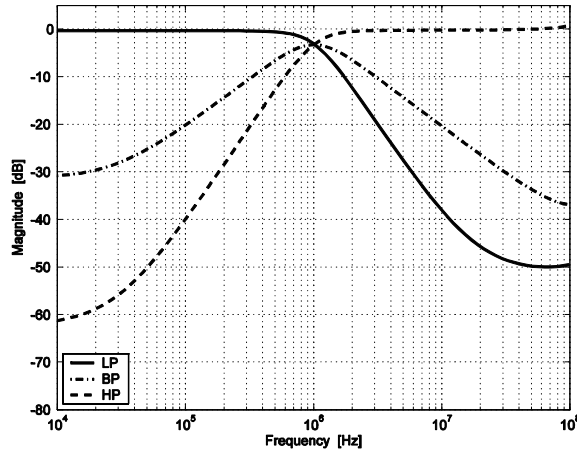


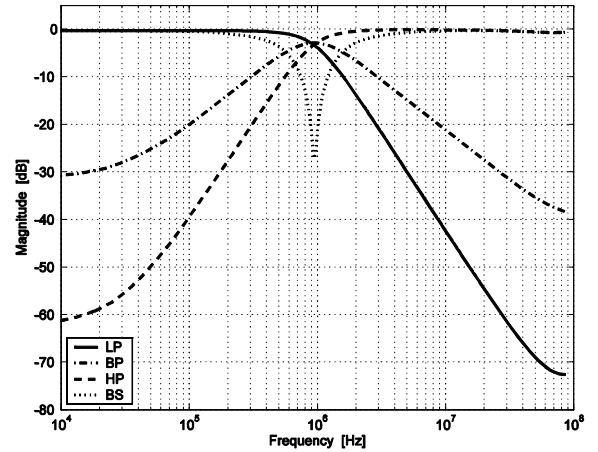
Fig. 4 The CMOS circuit of the DVCC [14].

Table III. Aspect ratios of MOS transistors of DVCC in Fig. 4 [14]

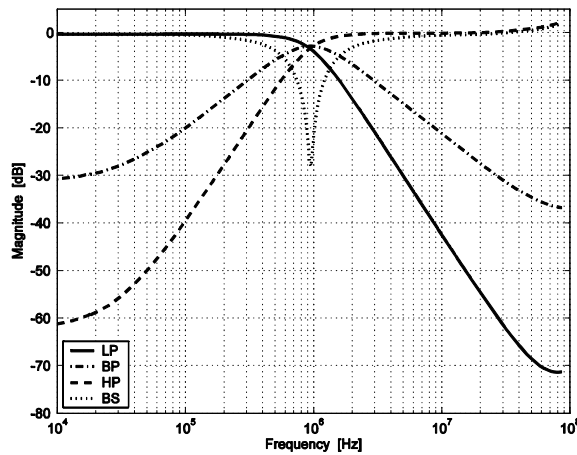
NMOS transistors	W [μm] / L [μm]
M1, M2, M3, and M4	25/0.5
M5 and M6	8/0.5
M11 and M12	20/2.5
PMOS transistors	W [μm] / L [μm]
M7 and M8	10/0.5
M9 and M10	40/2



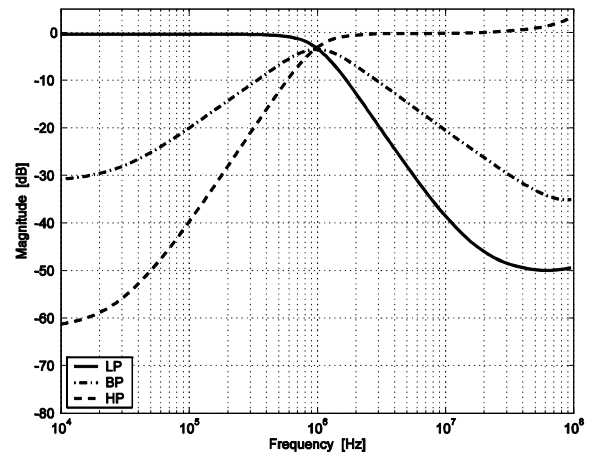
a)



b)



c)



d)

Fig. 5 Magnitude characteristics of the a) A, b) B, c) C, d) D variant for $f_0 = 1 \text{ MHz}$, $Q = 0.707$.

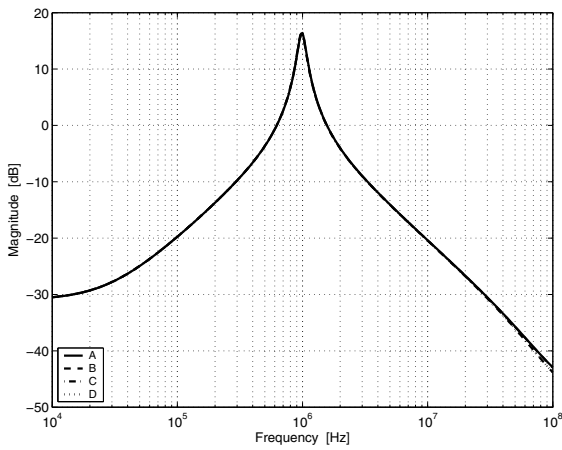


Fig. 6 Band-pass responses for $f_0 = 1$ MHz, $Q = 10$.

IV. CONCLUSION

The high input impedance current conveyor-based KHN circuit working in the voltage-mode employing four DVCC with single current output Z and seven grounded passive elements has been presented. Using the generalized description of the DVCC 23 alternative solutions can be found. Here, four variants that use only positive current output Z have been proposed and analyzed. According to the Spice simulation results the behavior of the presented biquad agrees with the theoretical assumptions well.

ACKNOWLEDGMENT

The paper has been supported by the Czech Science Foundation project GACR 102/09/1681, and Ministry of Education of the Czech Republic project No. MSM0021630513.

REFERENCES

- [1] W. Kerwin, L. Huelsman, R. Newcomb, "State variable synthesis for insensitive integrated circuit transfer functions", *IEEE Journal of Solid State Circuits*, 1967, vol. SC-2, no. 3, pp. 87-92.
- [2] B. J. Maundy, A. R. Sarkar, S. J. Gift, "A New Design Topology for Low-Voltage CMOS Current Feedback Amplifiers", *IEEE Trans. Circuits and Systems II*, 2006, vol. 53, no. 1, pp. 34-38.
- [3] S.-H. Yang, K.-H. Kim, Y.-H. Kim, Y. You, K.-R. Cho, "A Novel CMOS Operational Transconductance Amplifiers Based on a Mobility Compensation Technique", *IEEE Trans. Circuits and Systems II*, 2005, vol. 52, no. 1, pp. 37-42.
- [4] S. BenSalem, M. Fakhfakh, M. Loulou, N. Masmoudi, "An Improved High Performance CMOS Second Generation Current Conveyor", *IEEE Circuits and Systems, Proc. ISSCS 2005*, vol. 2, pp. 693-696.
- [5] I. M. Filanovsky, "CMOS voltage conveyors, *Proc. of the 44th IEEE Midwest Symposium on Circuits and Systems 2001*, vol. 1, pp. 318-321.
- [6] T. Dostal, "High frequency state-variable biquadratic active filters", *Radioengineering*, 1998, vol. 7, no. 1, pp. 1-6.
- [7] S. Shah, D. R. Bhaskar, "Design of KHN biquad using operational transconductance amplifier", *IEEE Circuits and Systems, Proc. MWSCAS 2002*, pp. I- 48-51.
- [8] E. Altuntas, A. Toker, "Realization of voltage and current mode KHN biquads using CCCIs", *Int. J. Electron. Commun. (AEÜ)*, 2002, vol. 56, pp. 45-49.
- [9] M. A. Ibrahim, S. Minaei, H. Kuntman, "A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements," *Int. J. Electron. Commun. (AEÜ)*, 2005, vol. 59, pp. 313-318.
- [10] J. Koton, K. Vrba, N. Herencsár, "Variable Q and ω_0 multifunction filter using Universal Voltage Conveyors", In *2009 RISP Int. Workshop on Nonlinear Circuits and Signal Proc.*, March 2009, Hawaii.
- [11] M. Bhusan, R. W. Newcomb, "Grounding of capacitors in integrated circuits", *Electronics Letters*, 1967, vol. 3, pp. 148-149.
- [12] S. Minaei, M. A. Ibrahim, "A mixed-mode KHN-biquad using DVCC and grounded passive elements suitable for direct cascading", *Int. J. Circ. Theor. Appl.* (2008), doi: 10.1002/cta.493, (published online).
- [13] A. M. Soliman, "Generation and classification of Kerwin-Huelsman-Newcomb circuits using the DVCC", *Int. J. Circ. Theor. Appl.* (2008), doi: 10.1002/cta.503, (published online).
- [14] A. M. Soliman, "Kerwin Huelsman Newcomb Filter Using Inverting CCIP", *J. of Active and Passive Electronic Devices*, 2008, vol. 3, pp. 273-279.
- [15] H. O. Elwan, A. M. Soliman, "A novel CMOS differential voltage current conveyor and its applications", *IEE Proc. Circuits, Devices and Systems*, 1997, vol. 144, no. 3, pp. 195-200.